
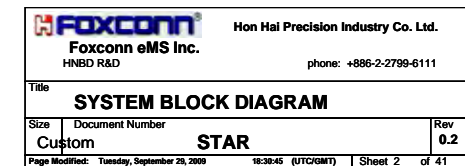
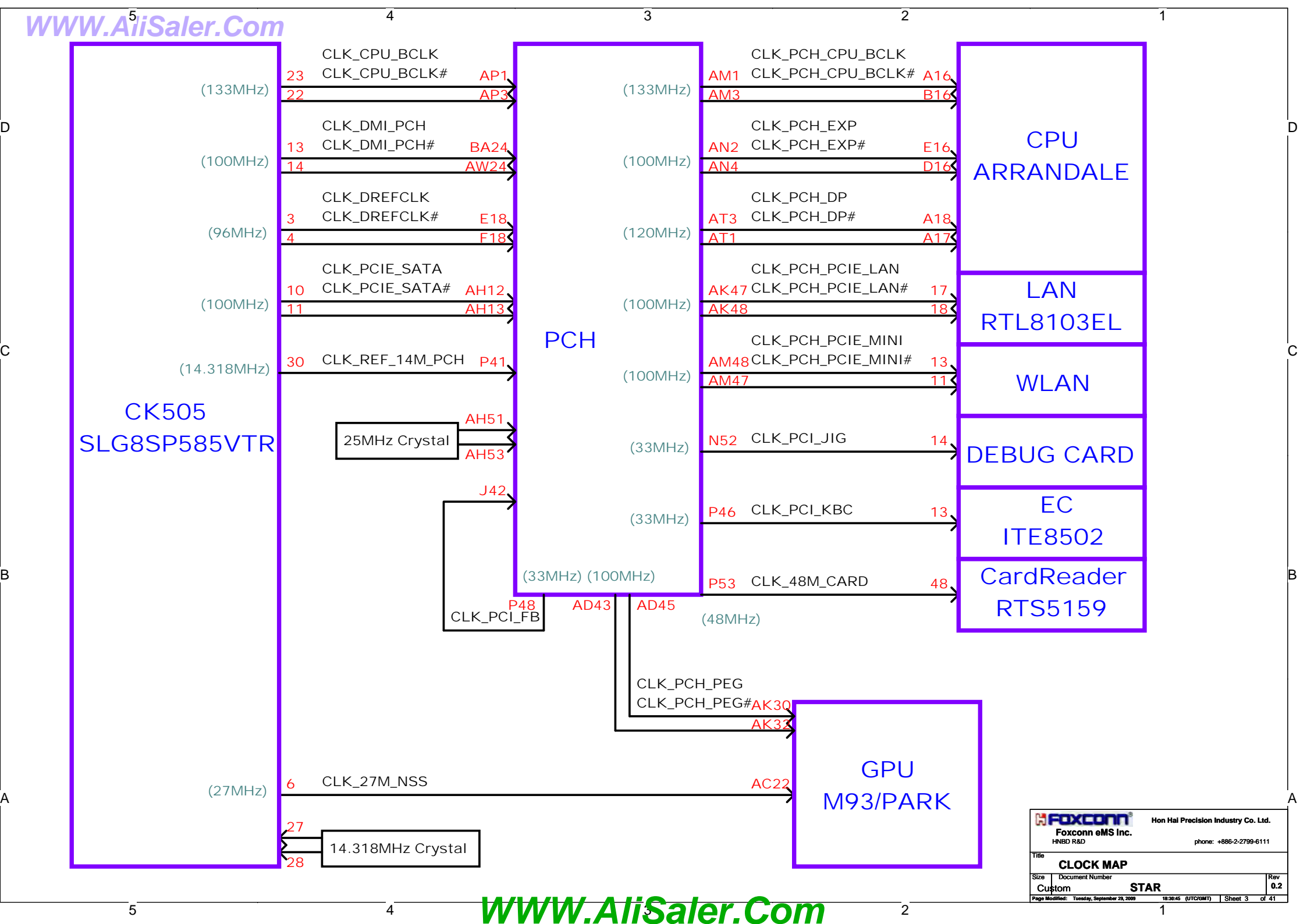


01 -- COVER SHEET	21 -- VGA_S3 (IO) 2/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DDR3) 3/5
03 -- CLOCK MAP	23 -- VGA_S3 (DP) 4/5
04 -- POWER MAP	24 -- VGA_S3 (POWER) 5/5
05 -- POWER SEQUENCY DIAGRAM	25 -- VRAM (DDR3)
06 -- POWER SEQUENCY TIMING	26 -- EC+KBC (IT8502E)
07 -- SMBUS MAP	27 -- CODEC/JACK/SPEAKER/MIC
08 -- RESET SIGNAL MAP	28 -- LAN (RTL8103EL)/CLOCK GEN
09 -- Calpella (DMI,PEG,FDI)	29 -- Card Reader
10 -- Calpella (CLK,MISC,JTAG)	30 -- WLAN/BT/MDC/USB/MOUNTING
11 -- Calpella (DDR3)	31 -- LVDS/CRT/Webcam
12 -- Calpella (POWER/GND)	32 -- HDMI
13 -- Calpella (GRAPHIC POWER)	33 -- DCIN/Battery/OCP/FAN
14 -- PCH (HDA,JTAG,SATA)	34 -- PWR_Charger MAX8731AETI
15 -- PCH (PCI-E,SMBUS,CLK)	35 -- 5V/3.3V SN0608098RHBT
16 -- PCH (DMI,FDI,GPIO,LVDS)	36 -- Vcore MAX17030
17 -- PCH (PCI,USB,NVRAM,GPIO)	37 -- 1.1V VTT/+V1.05RUN
18 -- PCH (POWER)	38 -- 1.5VDDR3+0.75V+V1.8RUN
19 -- DDR3(SO-DIMM_0&1)	39 -- PWR_Others power plane
20 -- VGA (PCI-E/STRAP) 1/5	40 -- CPU VREG & Decoupling
	41 -- ATVDD/+VPCIE

P. Leader	Check by	Design by

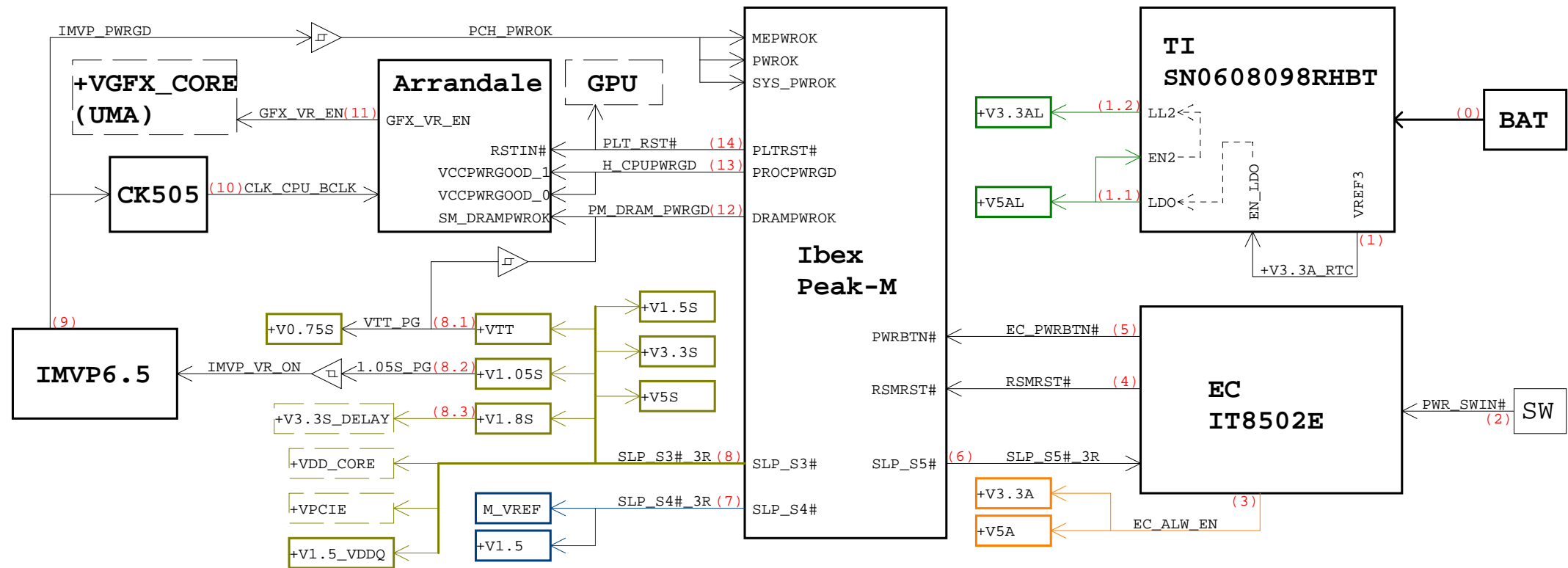
 Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D		phone: +886-2-2799-6111
Title Index Page		
Size Custom	Document Number STAR	Rev 0.2
Page Modified: Tuesday, September 29, 2009 18:30:43 (UTC/GMT) Sheet 1 of 41		







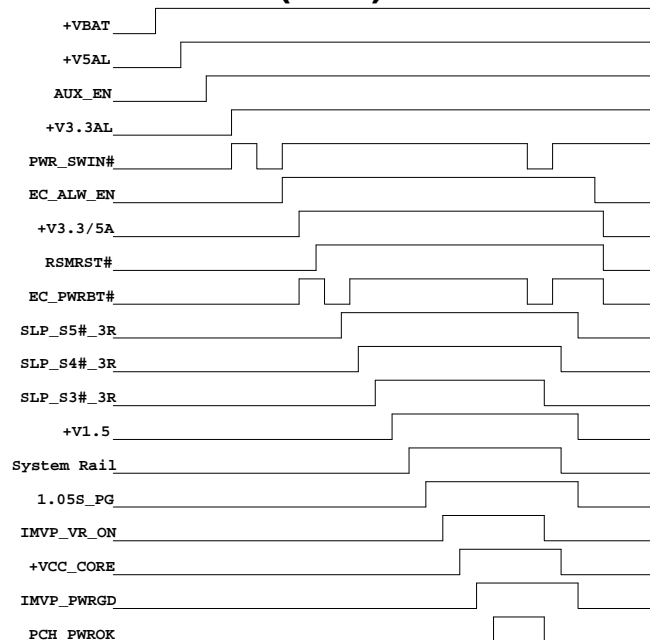
POWER SEQUENCY DIAGRAM



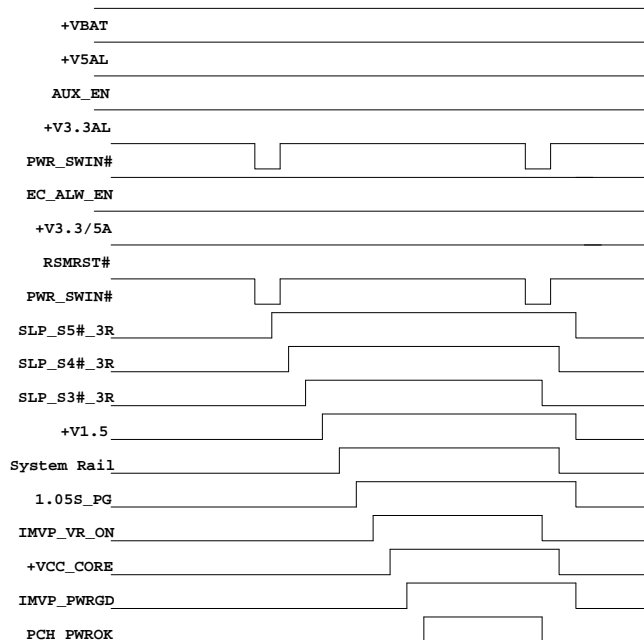
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

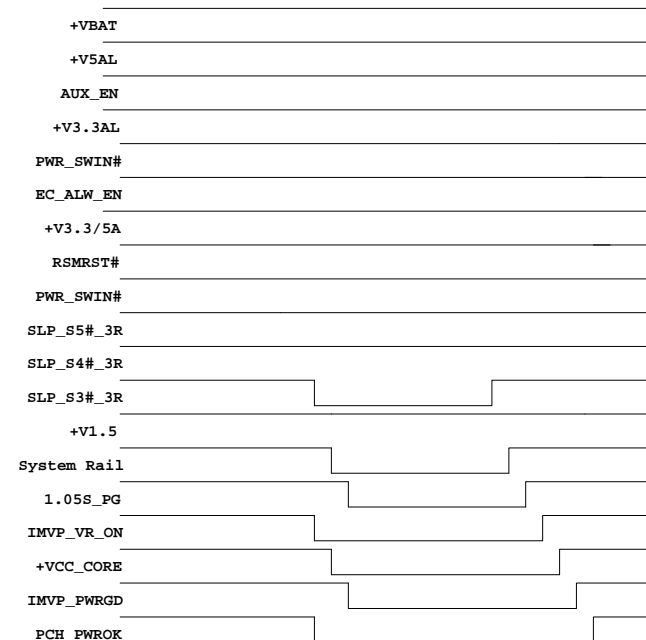
G3(OFF)->S0->S5



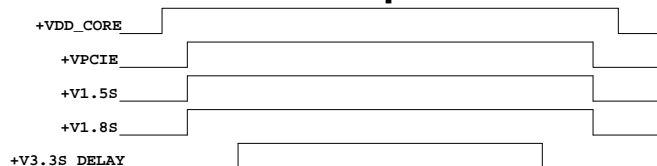
S5->S0->S5



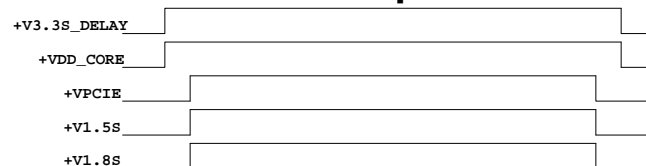
S0->S3->S0



M93 Sequence



Park Sequence



SMBUS&I2C MAP

Discrete
GPU

GPU
M93/Park
S3 Package

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN

WLAN

CRT

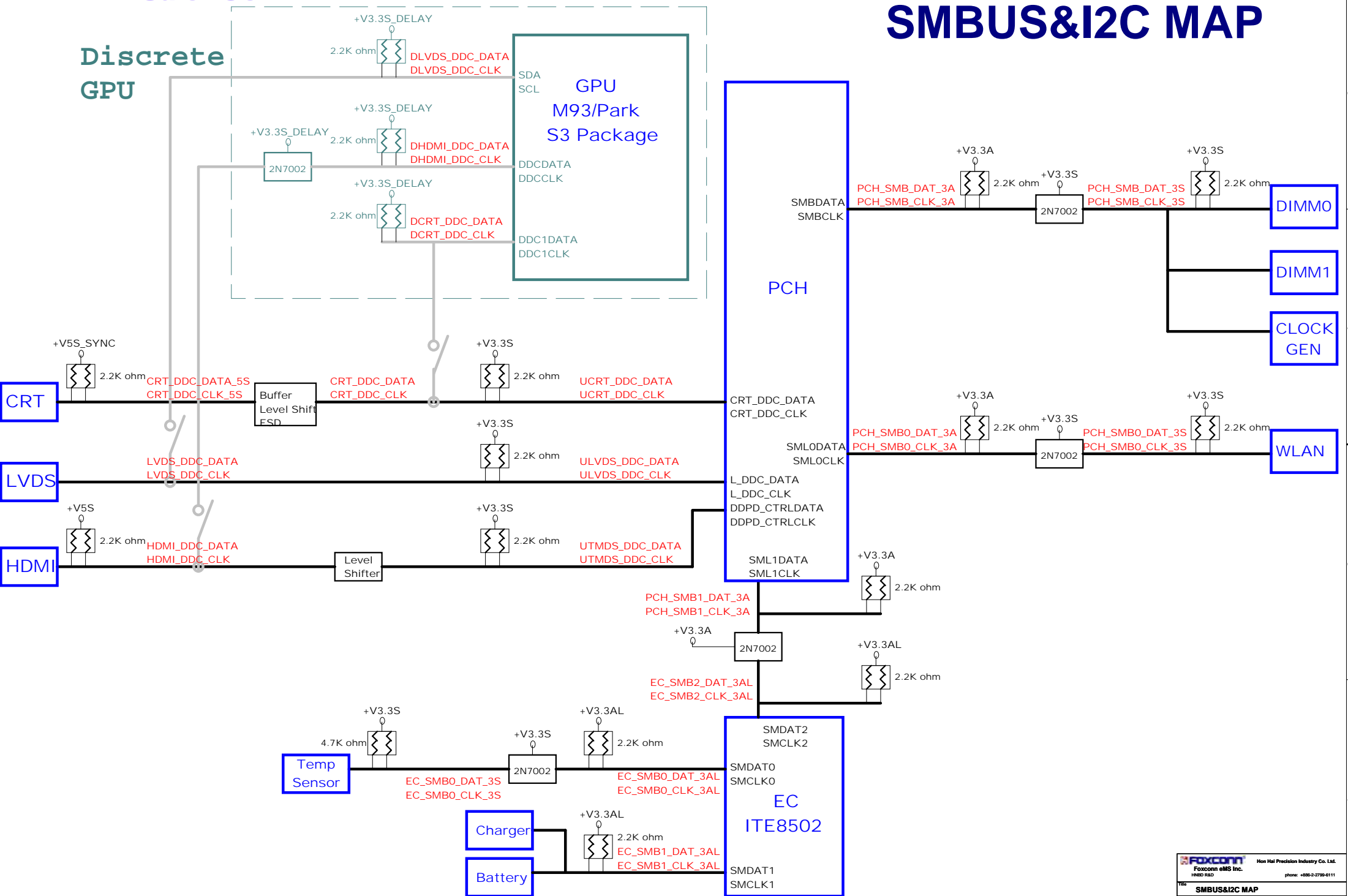
LVDS

HDMI


Temp
Sensor

Charger

Battery



RESET SIGNAL MAP



Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBD R&D

phone: +886-2-2799-6111

Title

RESET SIGNAL MAP

Size

Custom

Document Number

STAR

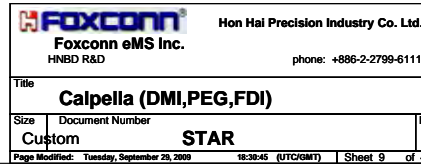
Rev

0.2

Page Modified: Tuesday, September 29, 2009

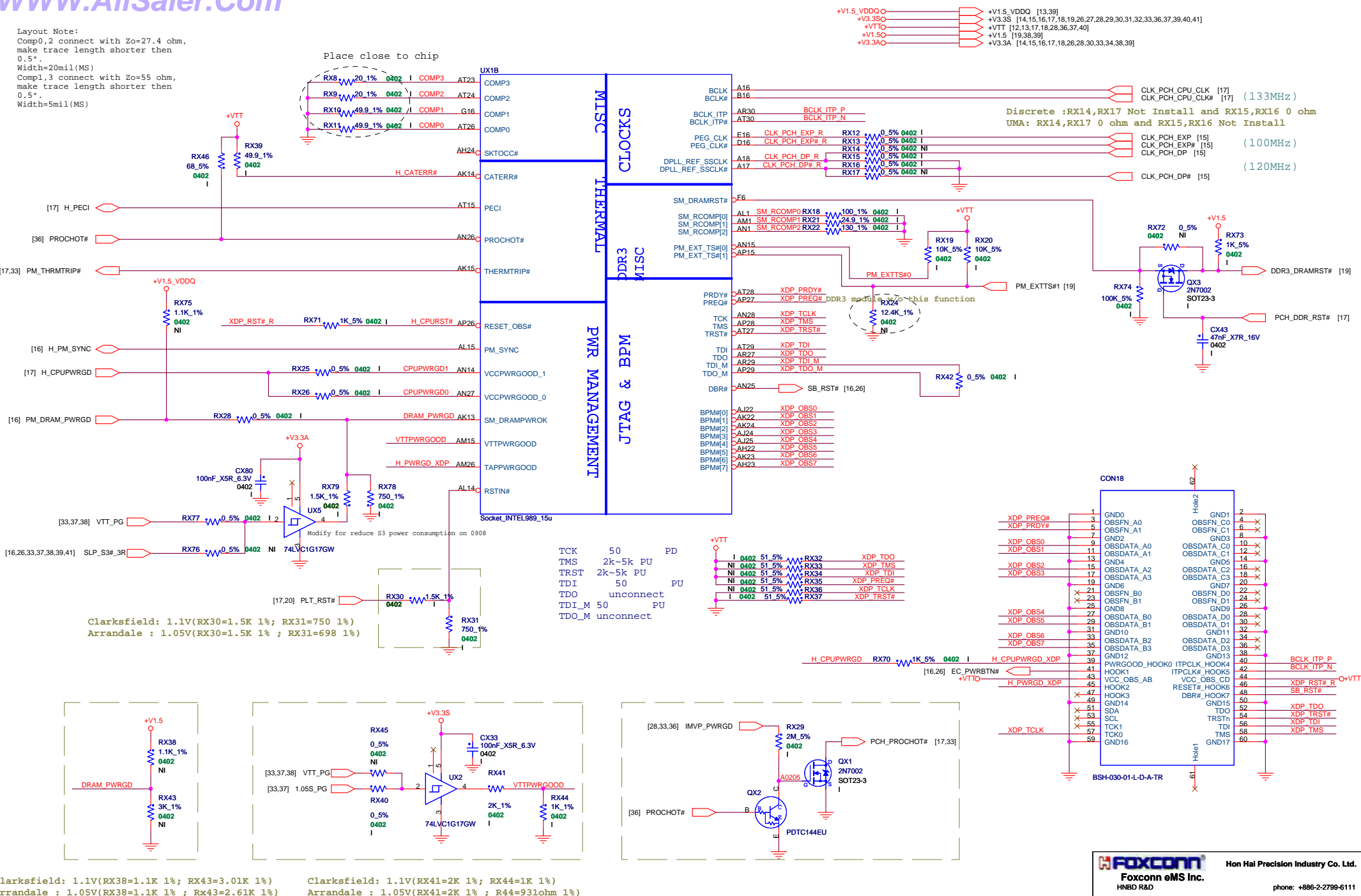
18:38:45 (UTC+8MT)

Sheet 8 of 41



Layout Note:
Comp0,2 connect with Zo=27.4 ohm,
make trace length shorter then
0.5".
Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm,
make trace length shorter then
0.5".
Width=5mil(MS)

Place close to chip

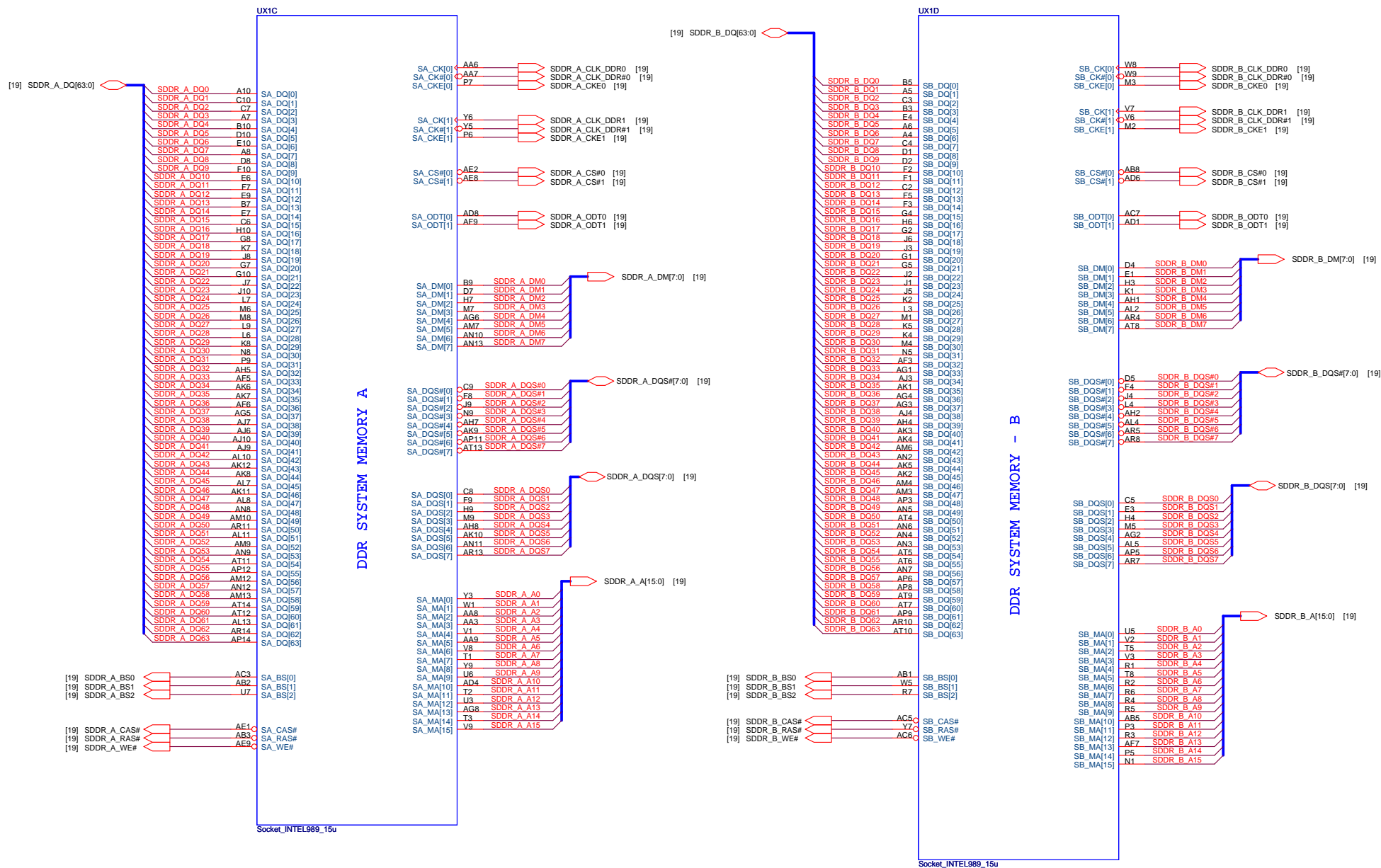


FOXCONN Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBD R&D
phone: +86-2-2799-6111

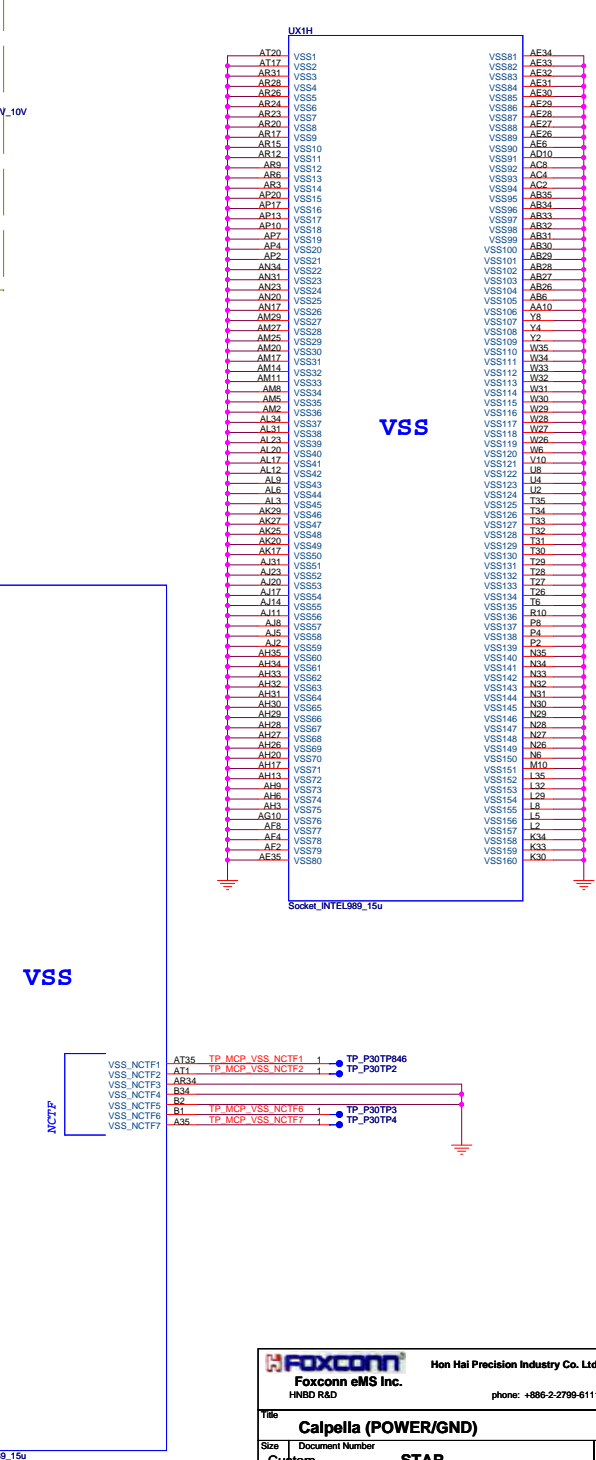
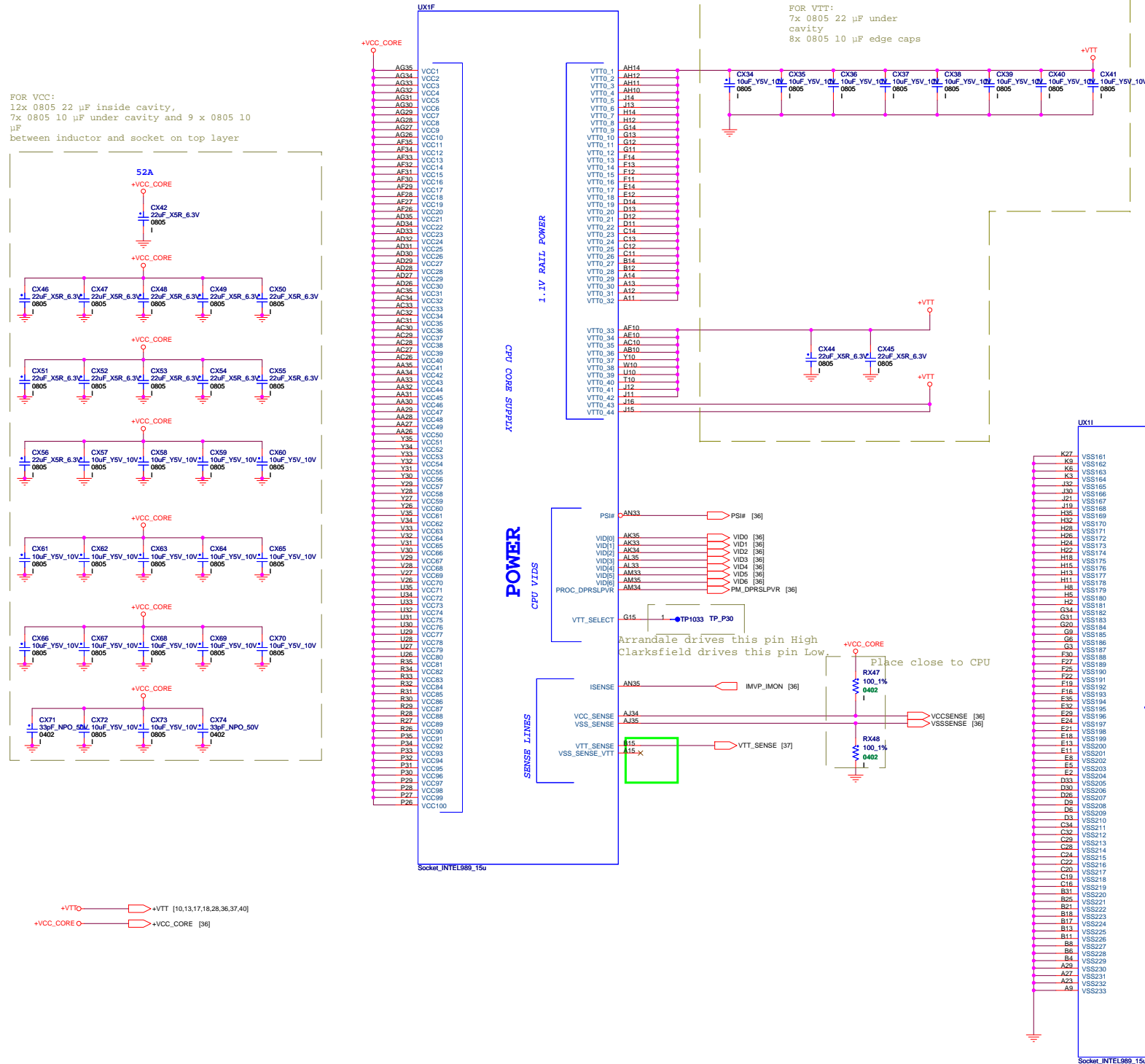
Title: **Calpella (CLK,MISC,JTAG)**

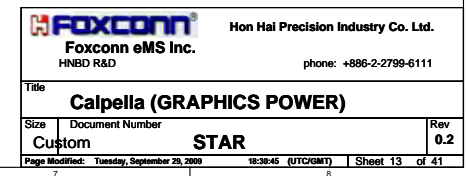
Size: Document Number
Custom: **STAR**
Page Modified: Tuesday, September 29, 2009 18:38:44 (UTC+8MT) Sheet 10 of 41

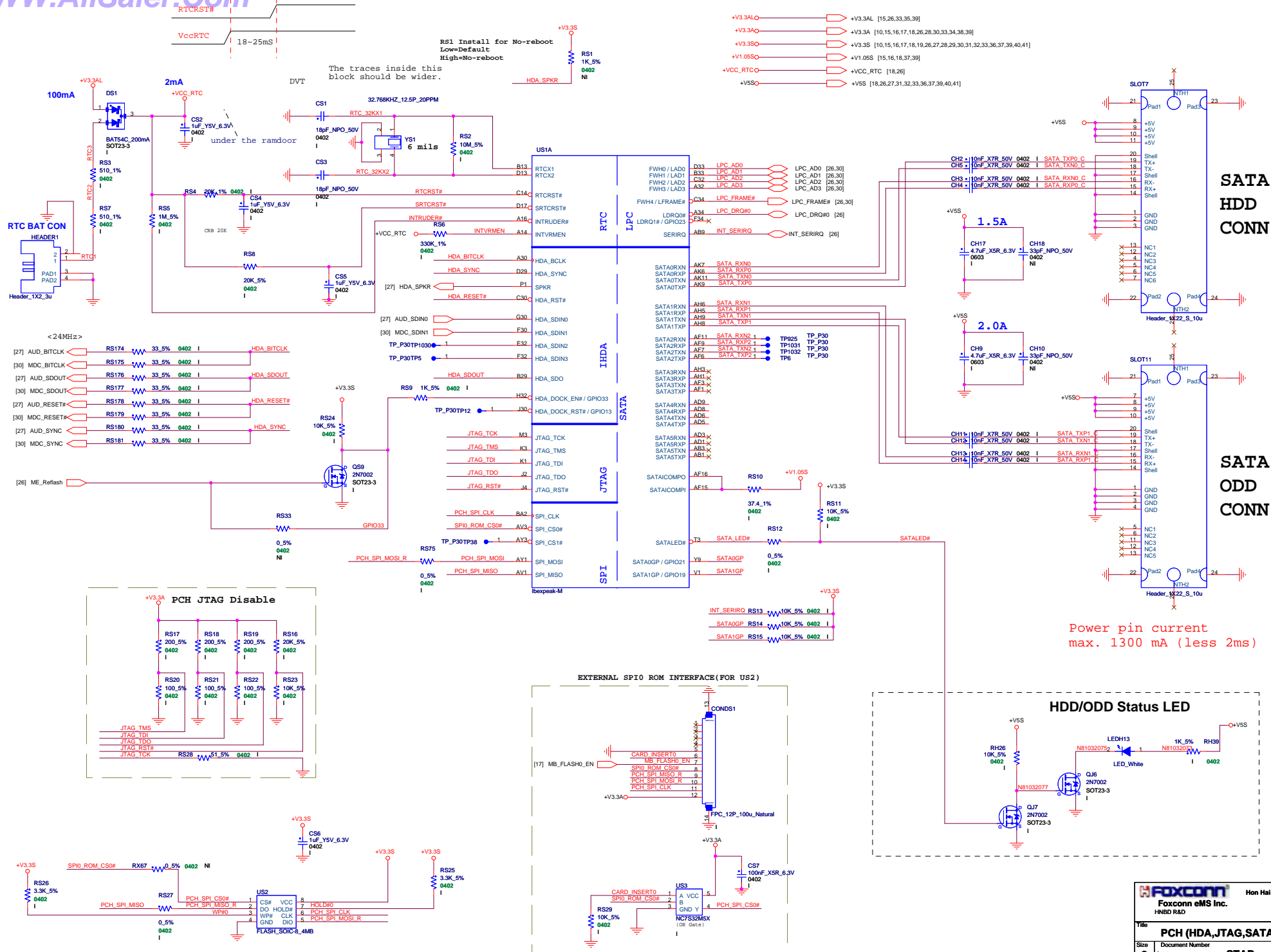
Rev: **0.2**

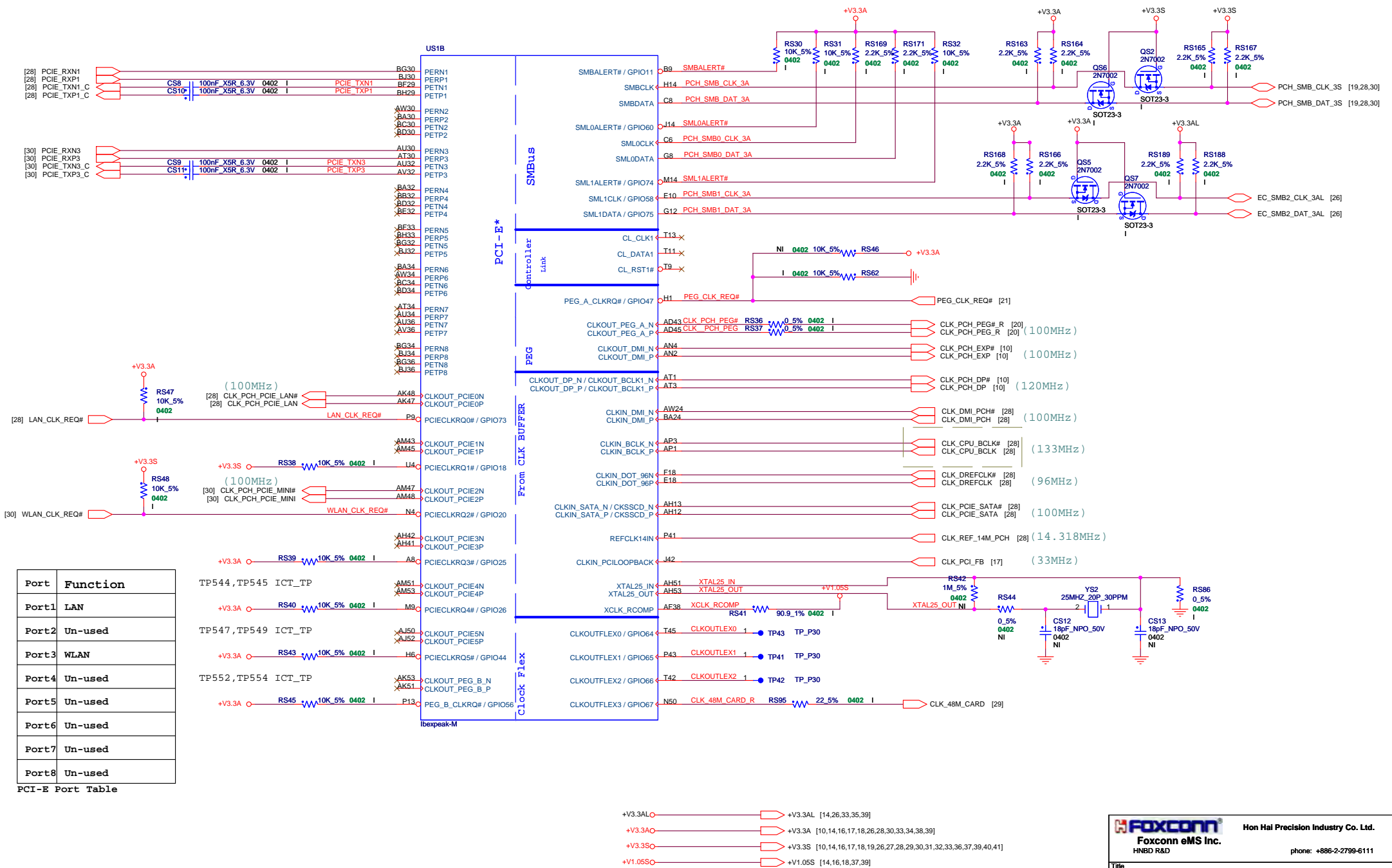


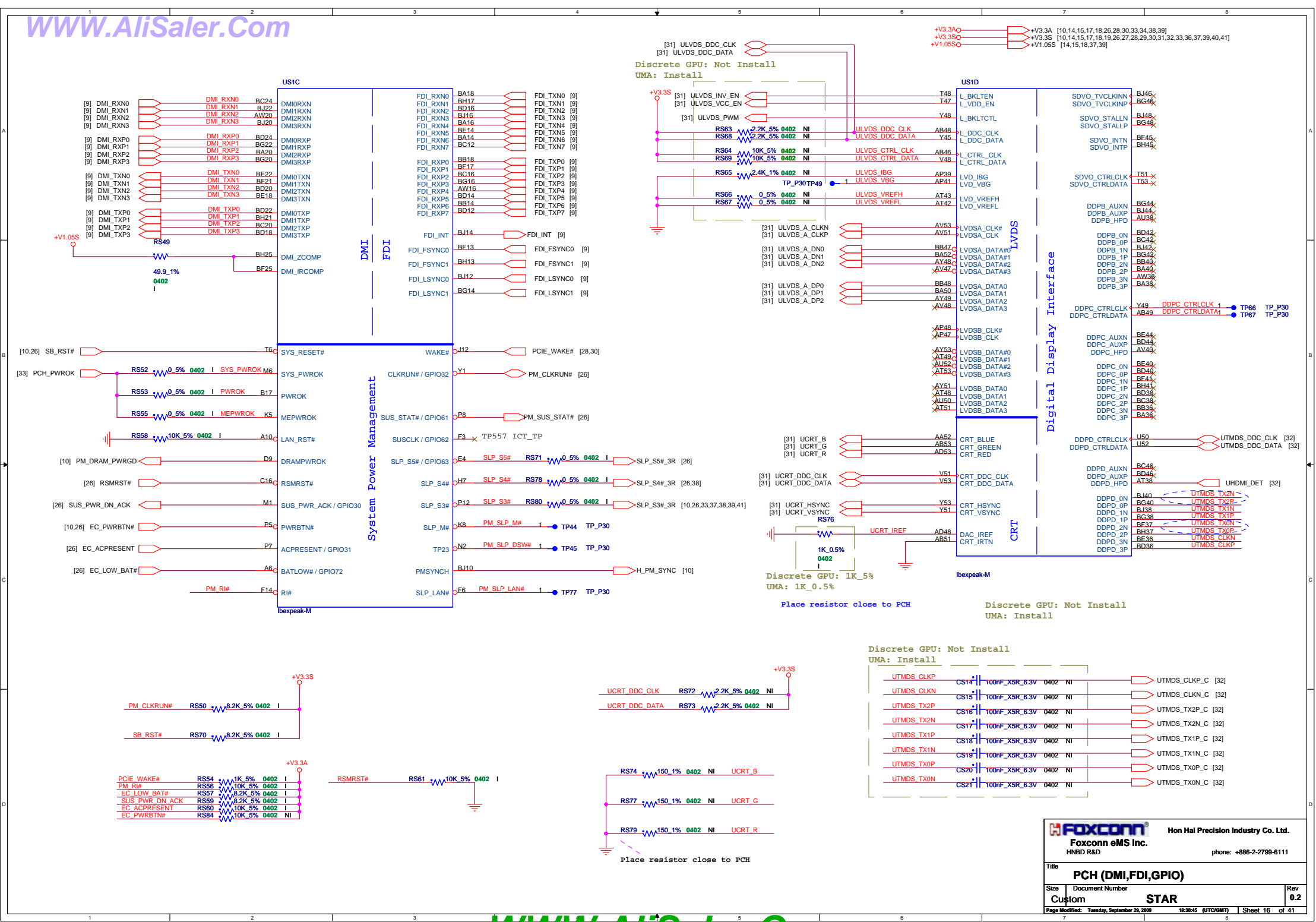
FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10
 μ F
between inductor and socket on top layer

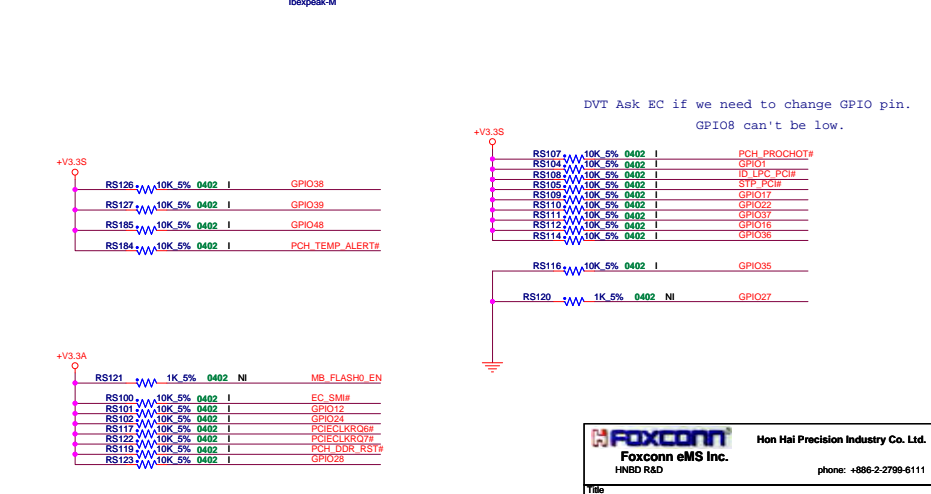
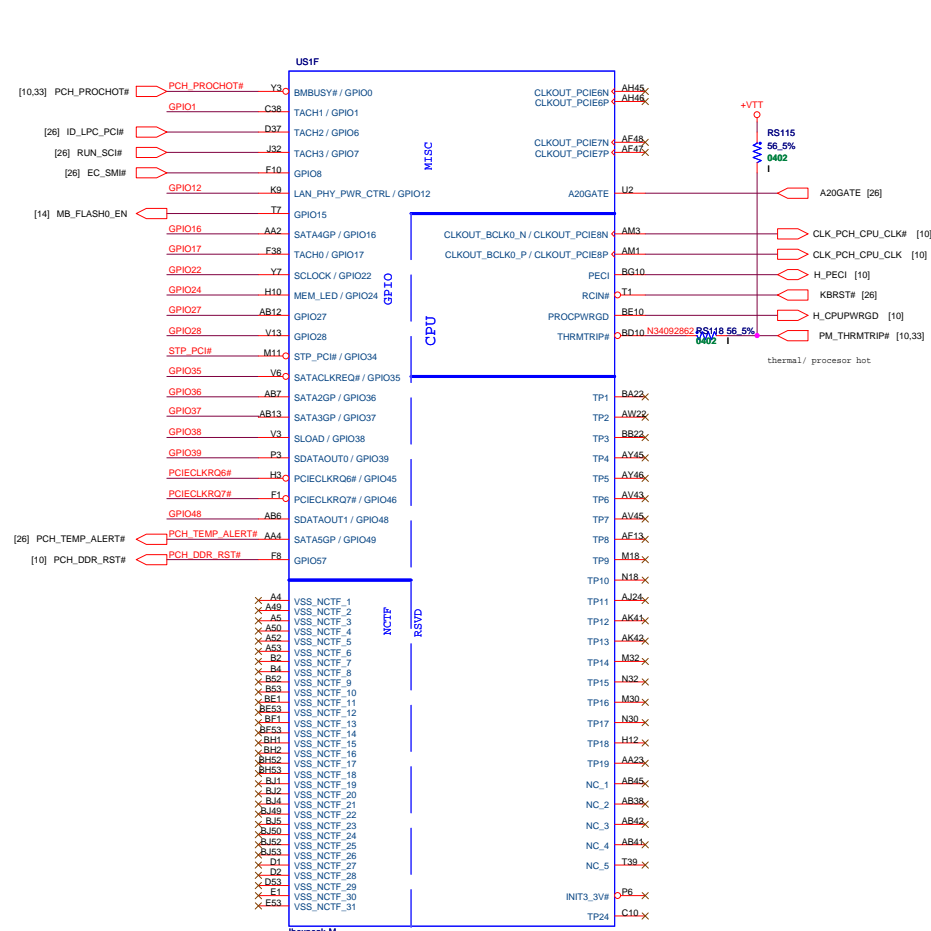
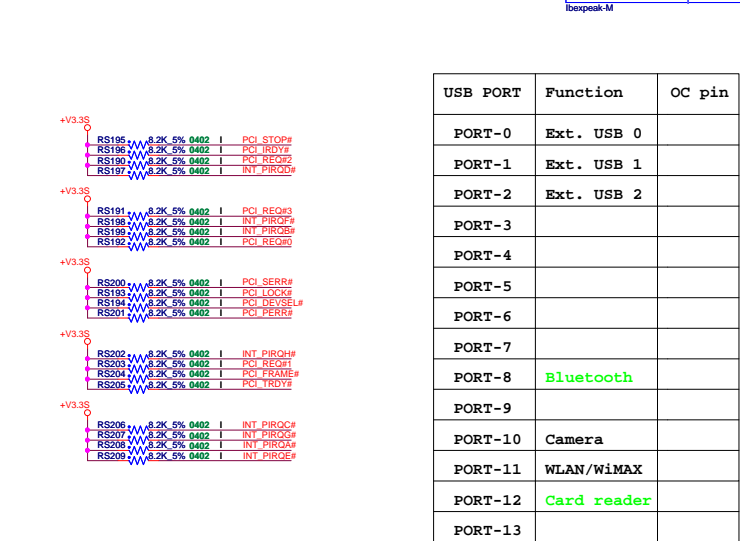
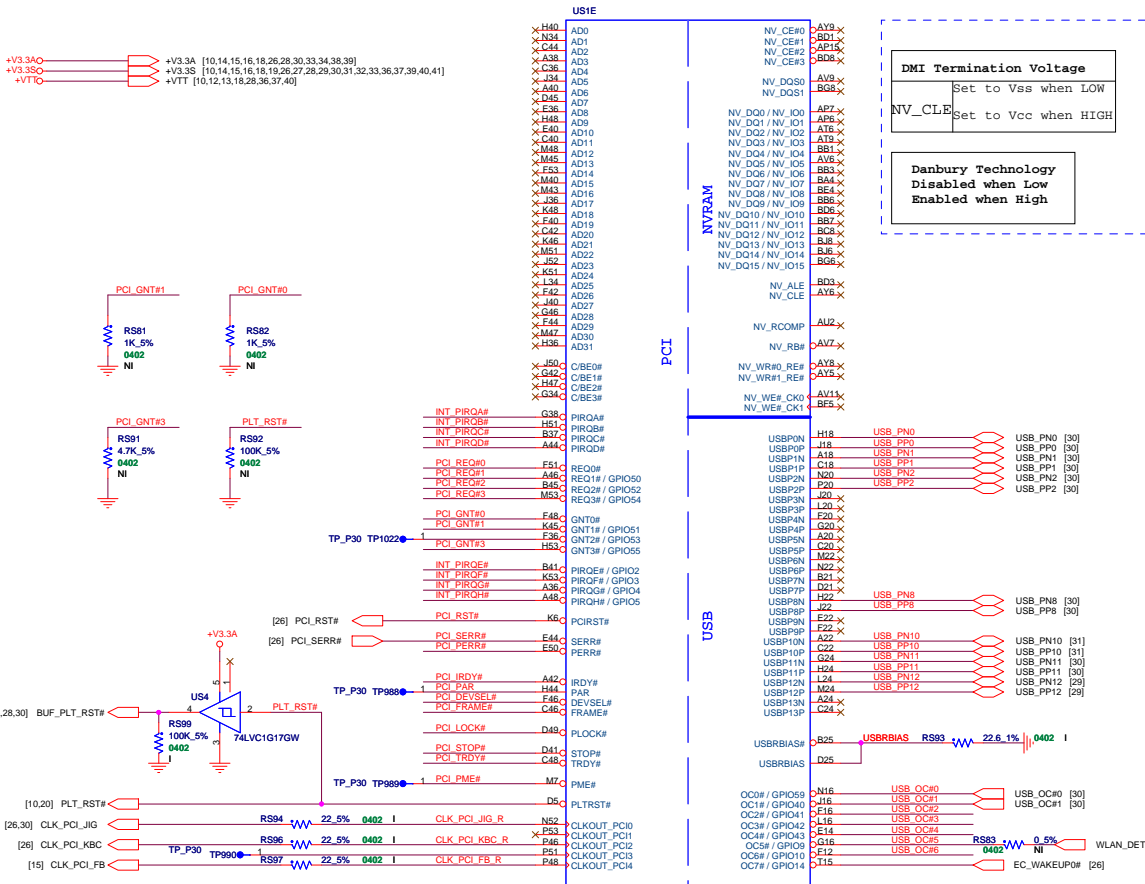


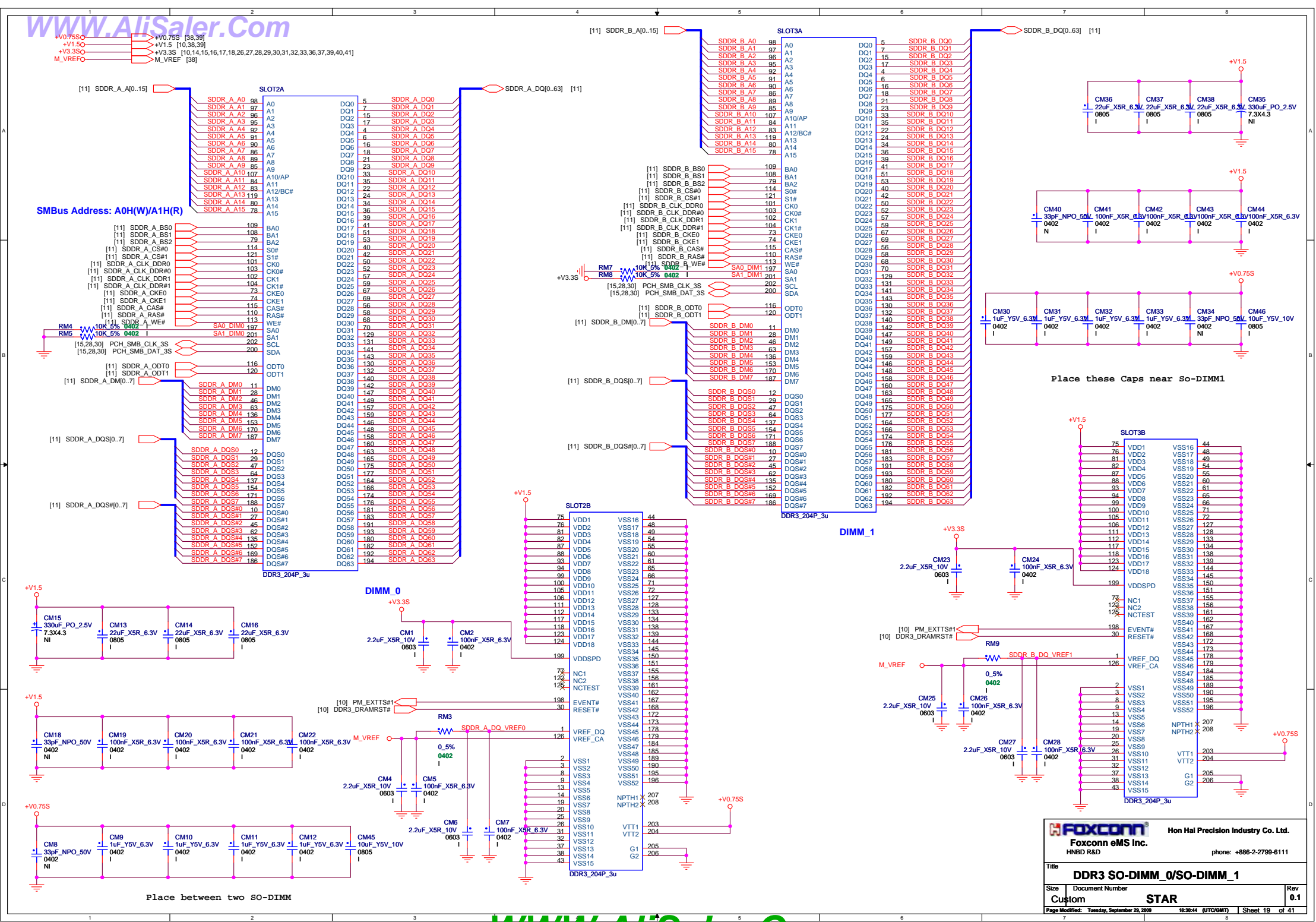


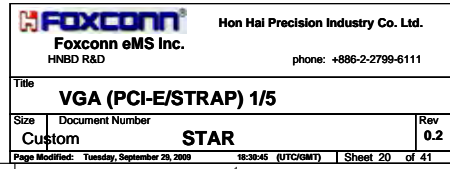


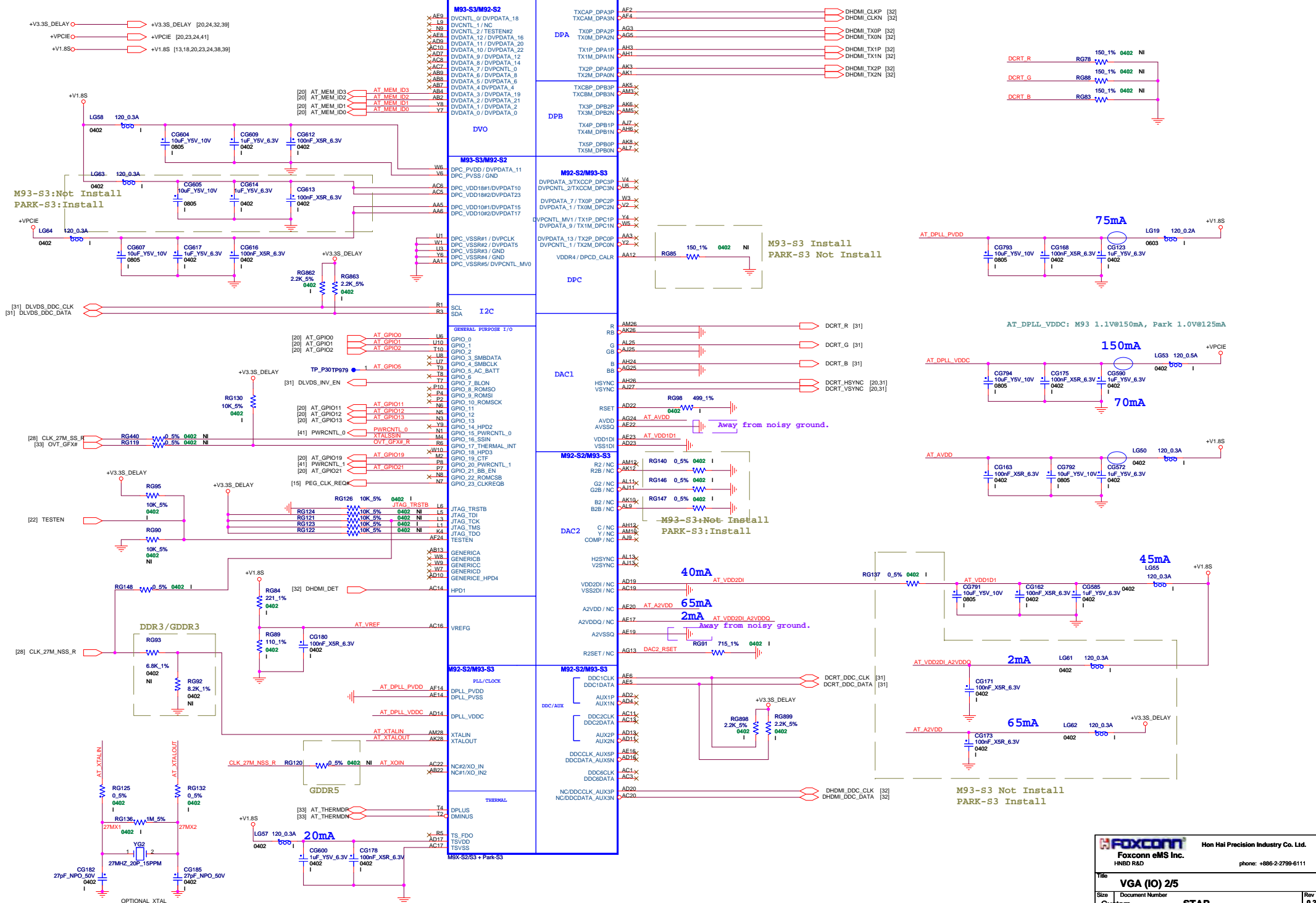


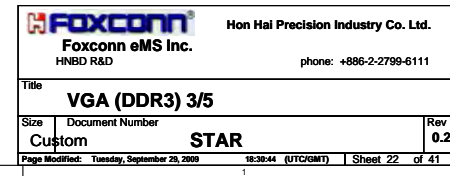


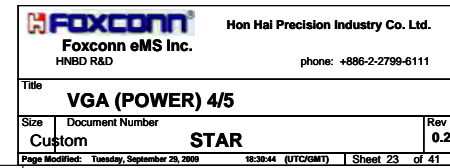


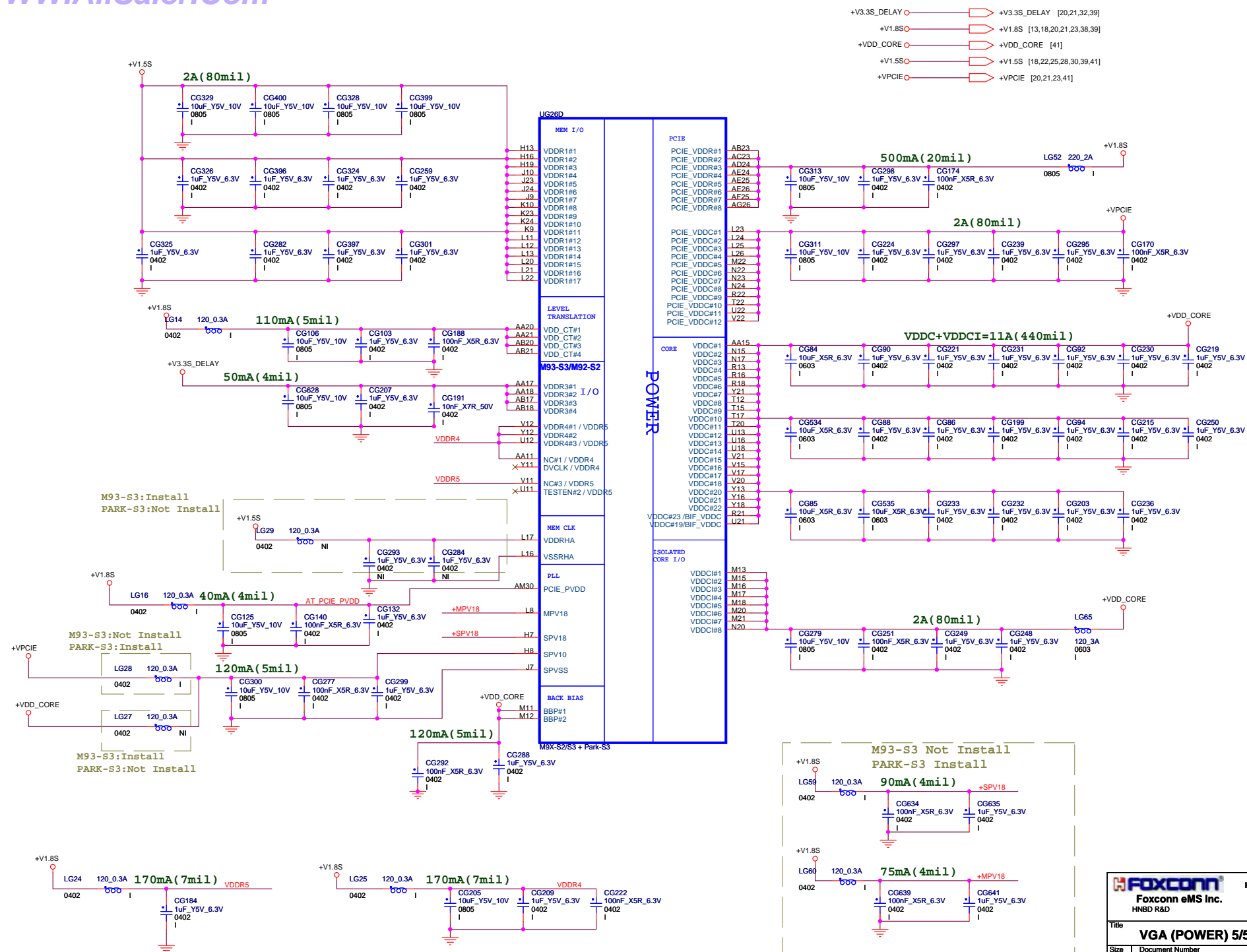




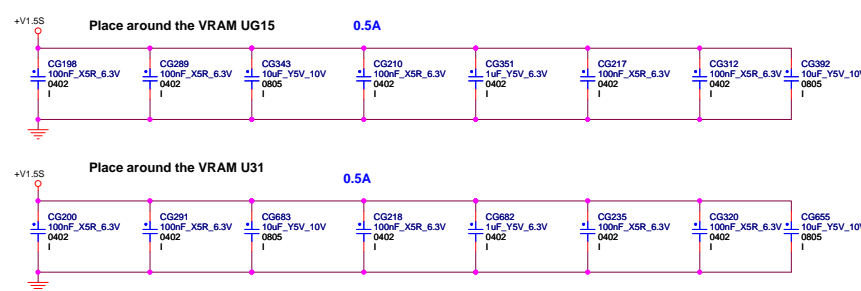
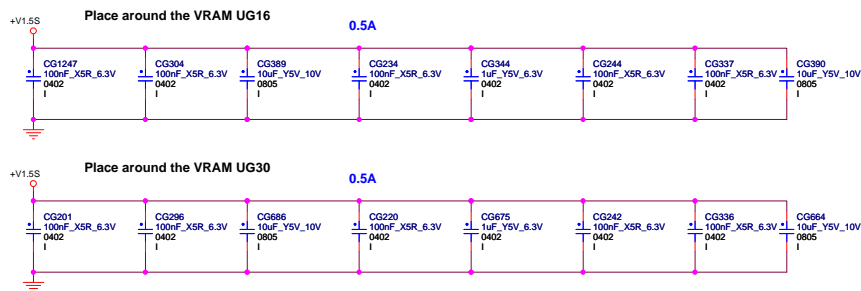
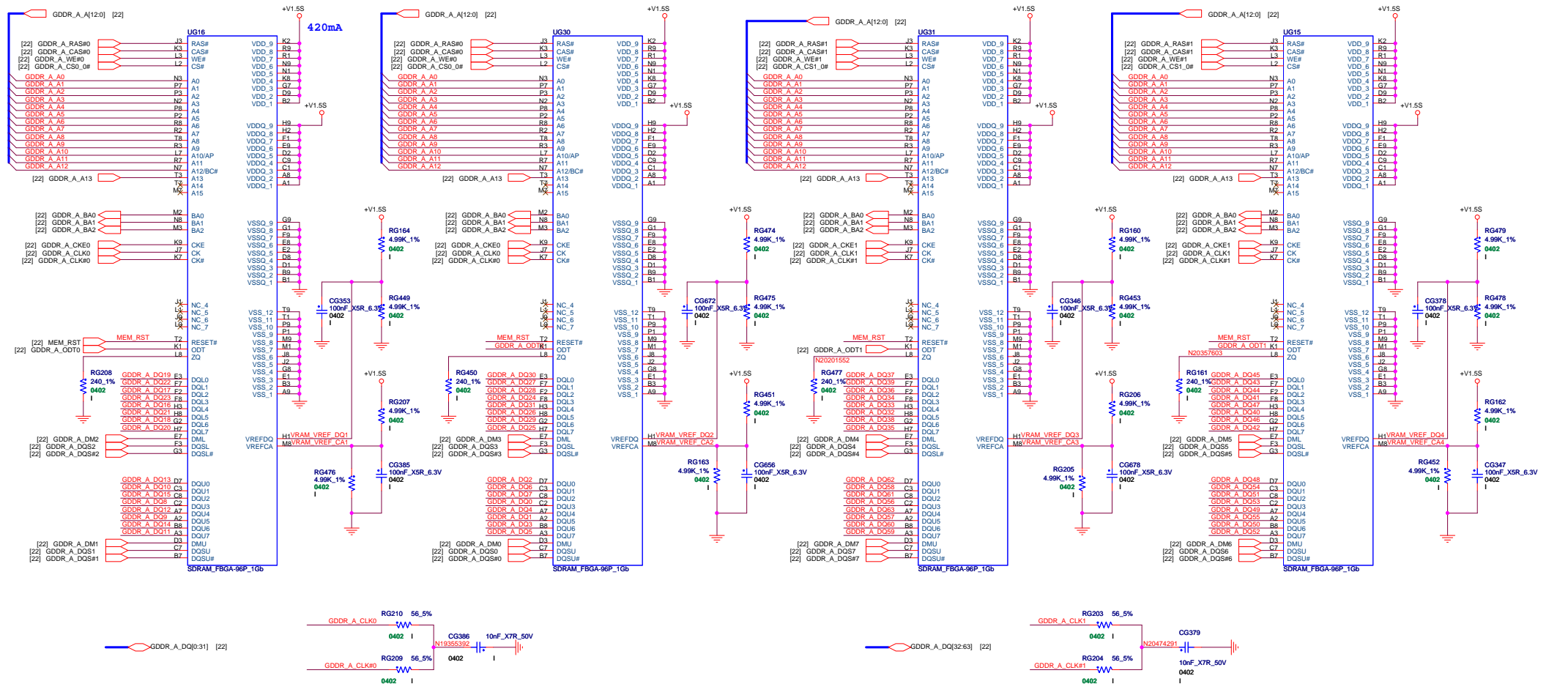


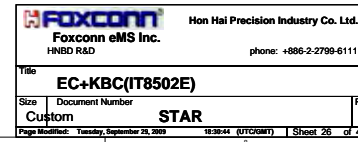


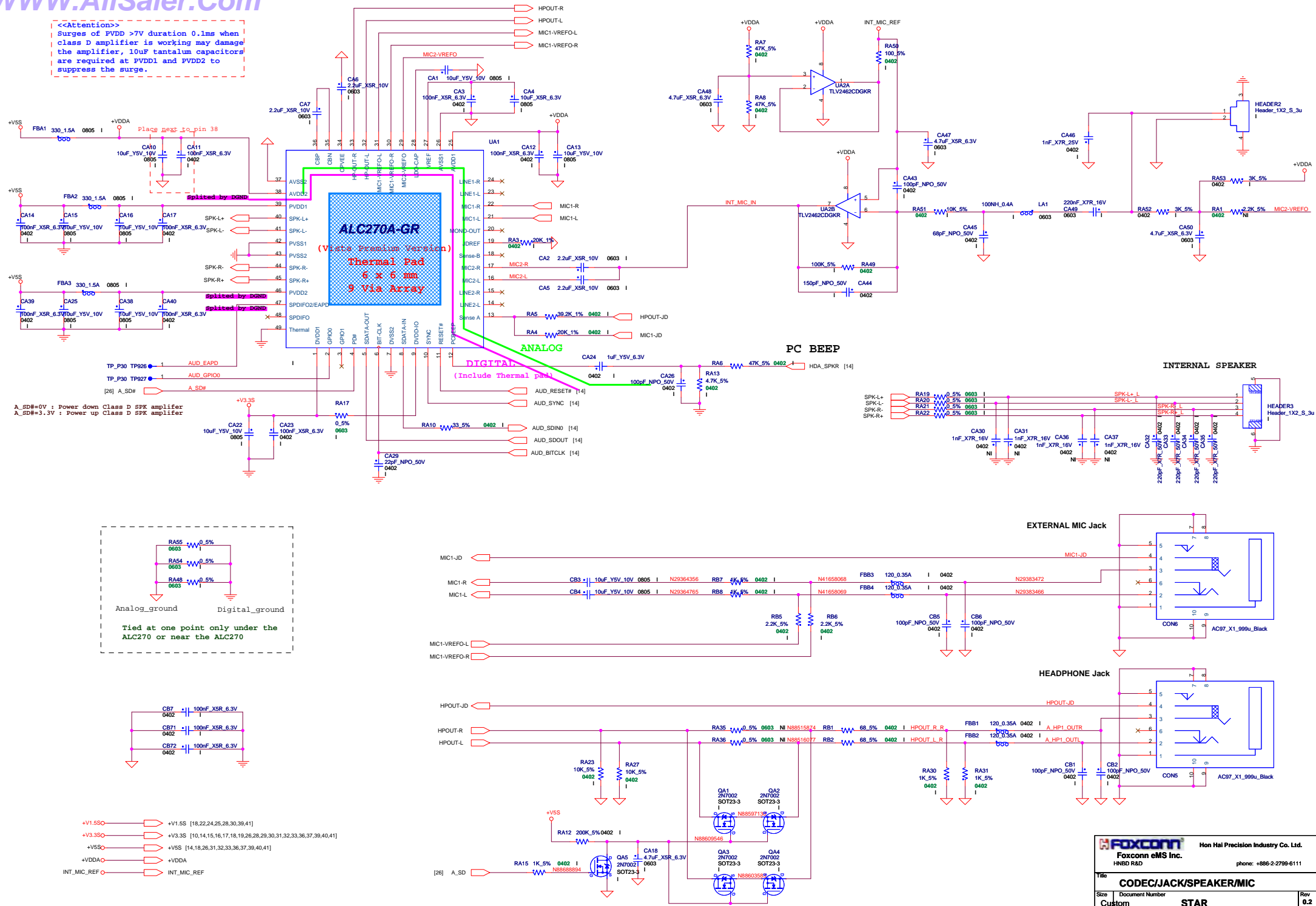


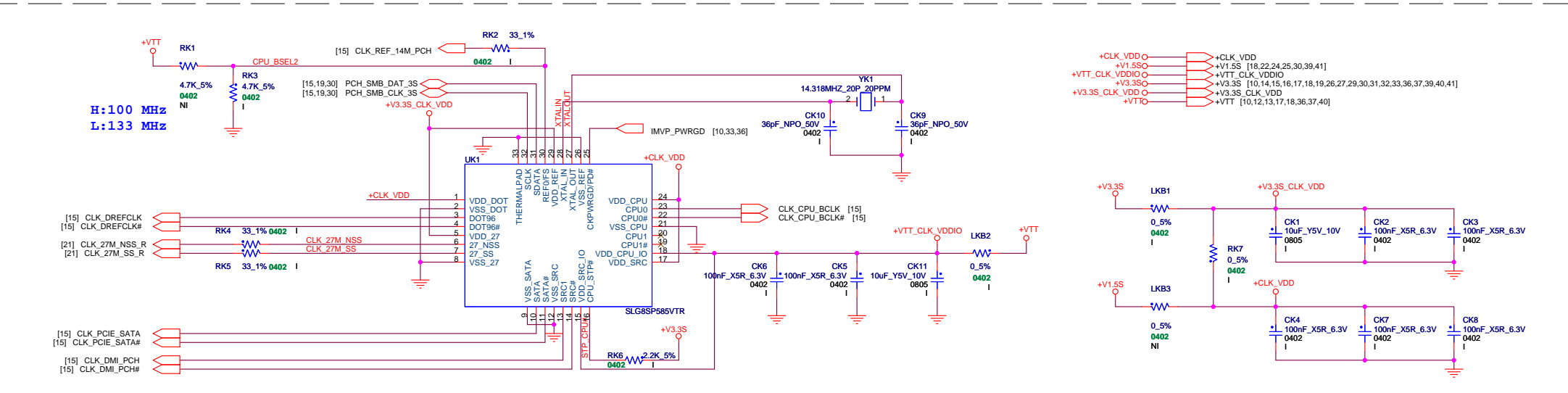
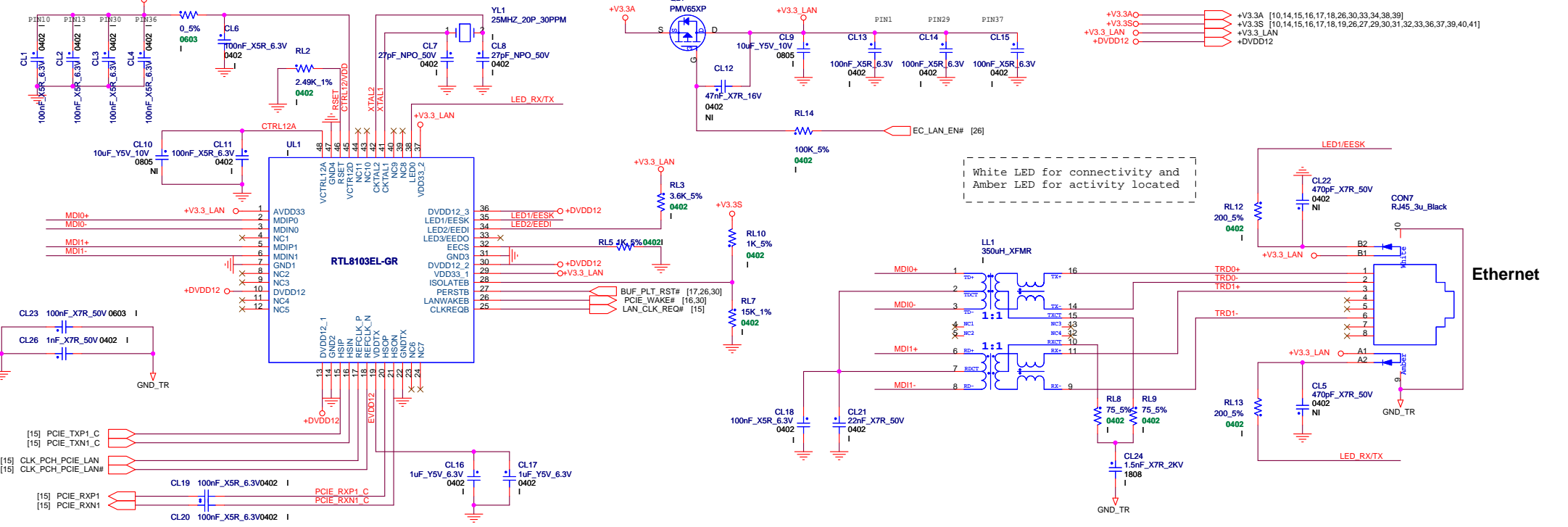


+V1.5S [18,22,24,28,30,39,41]





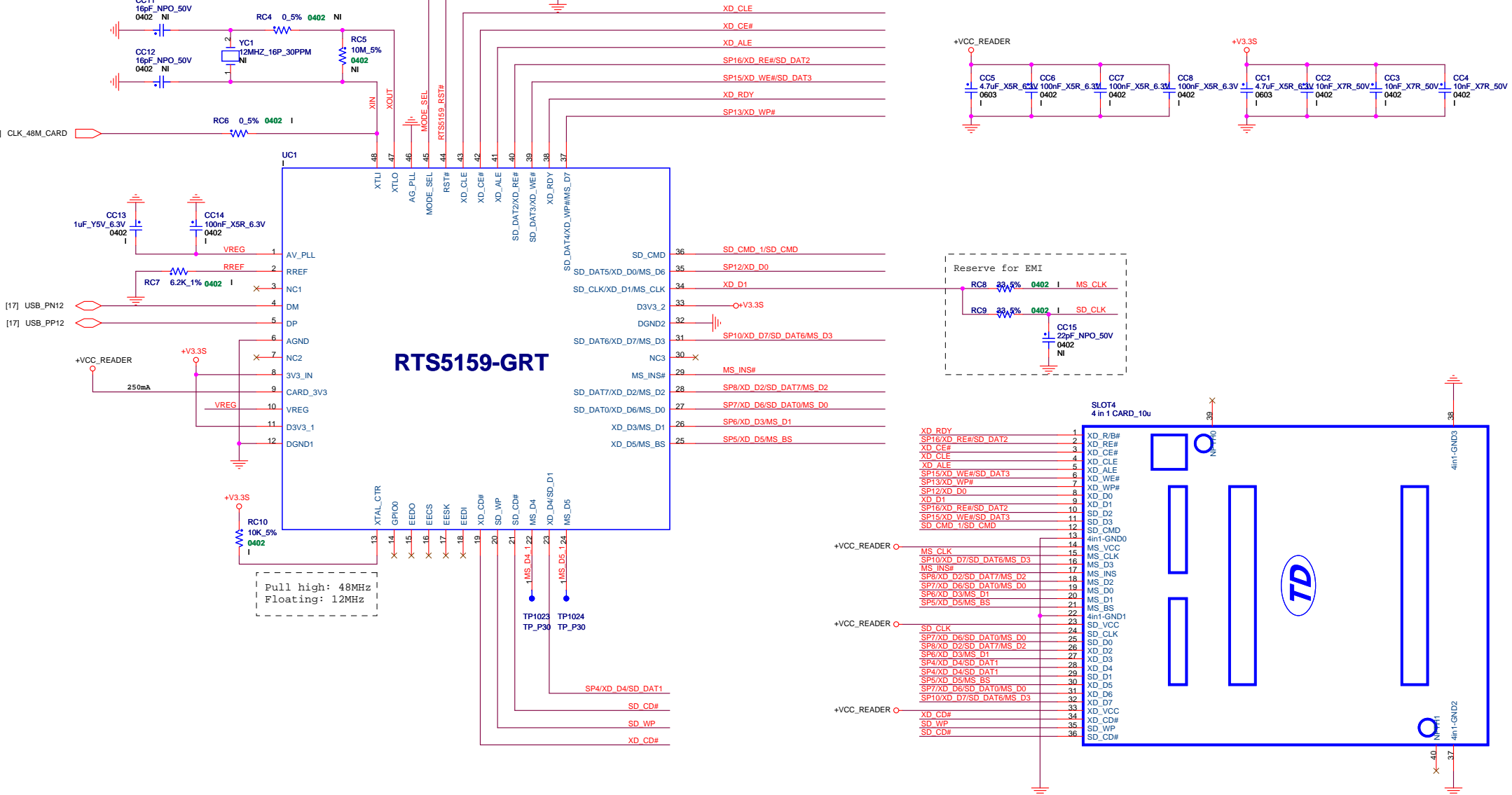




FSP Table

FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

D3 mode: (R:0 ohm ; C:NC)
If user remove memory card from socket, RTS5159 will terminate USB bus connection and enter D3 (power saving) state.





MDC CONN.



Bluetooth CONN.



USBX2 CONN.

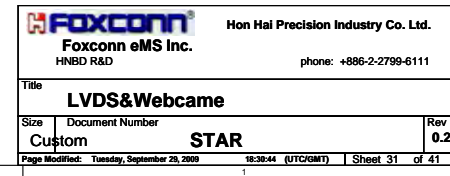


**MOUNTING
HOLE**

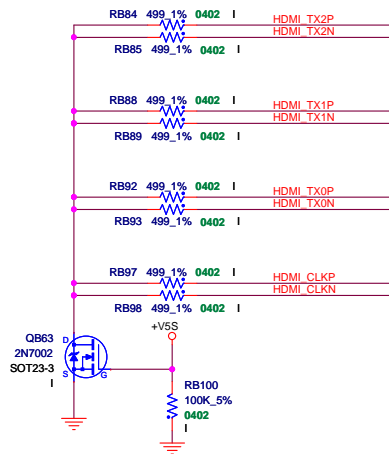
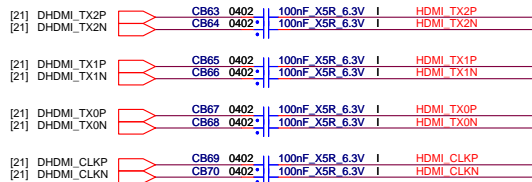
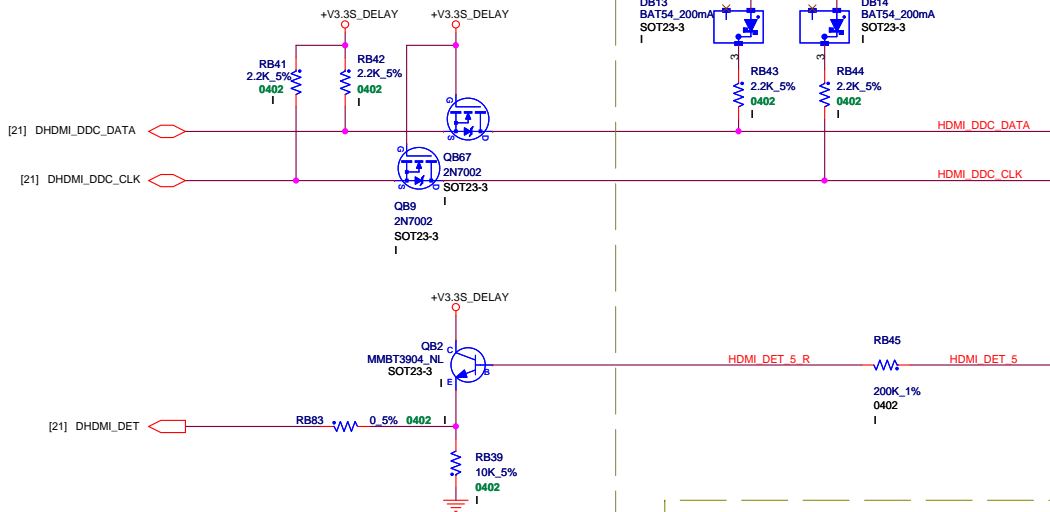


USBX1 CONN.

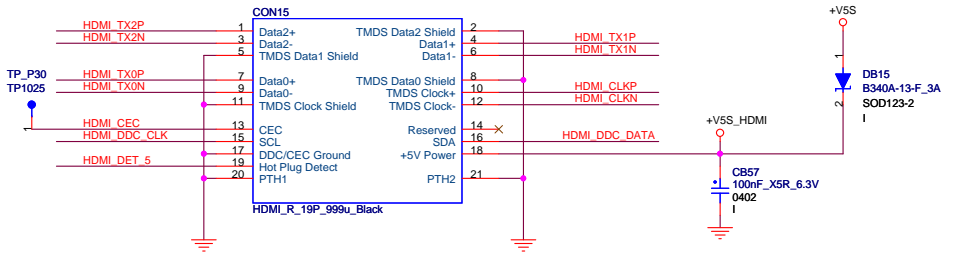
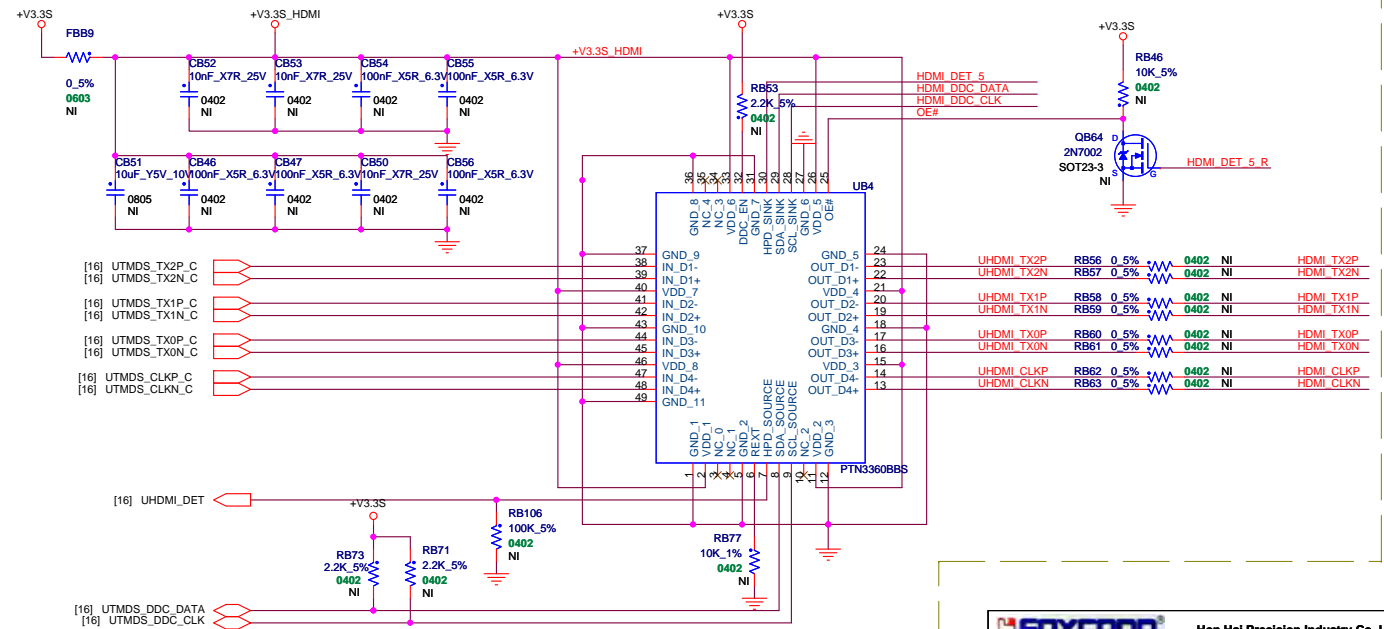


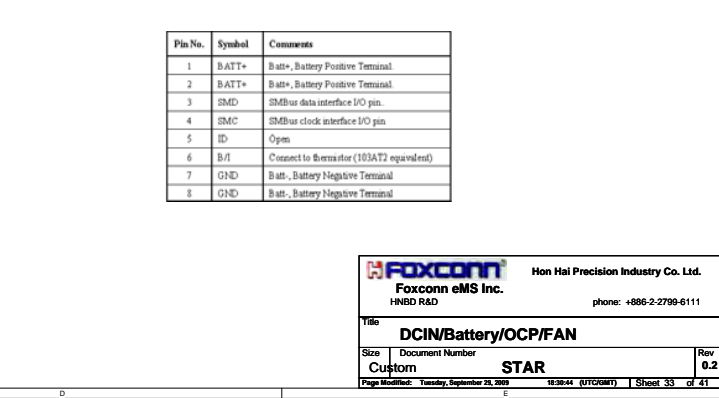
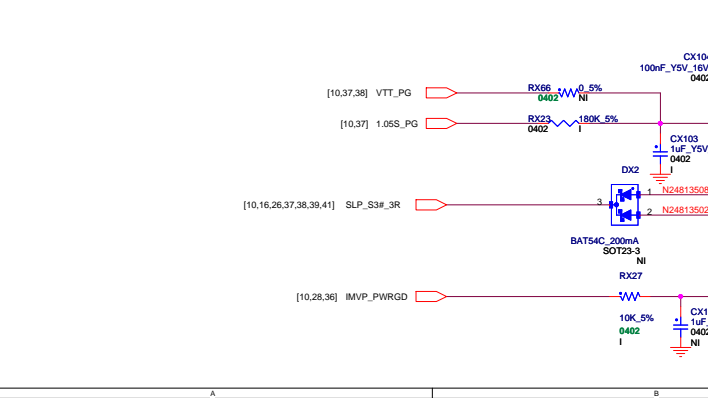
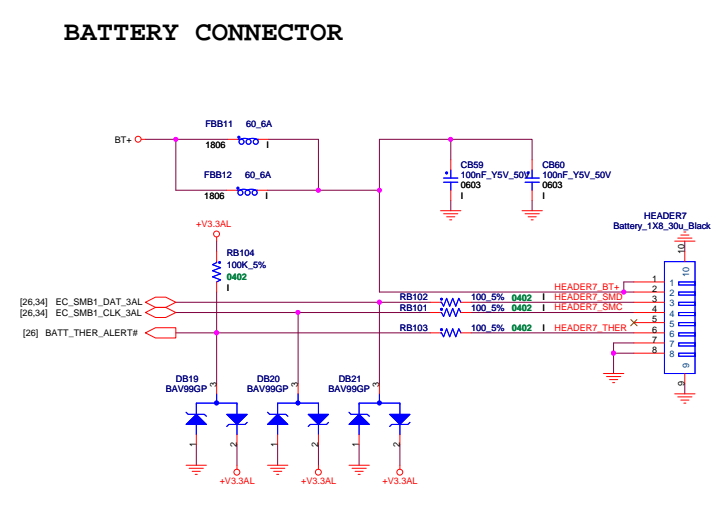
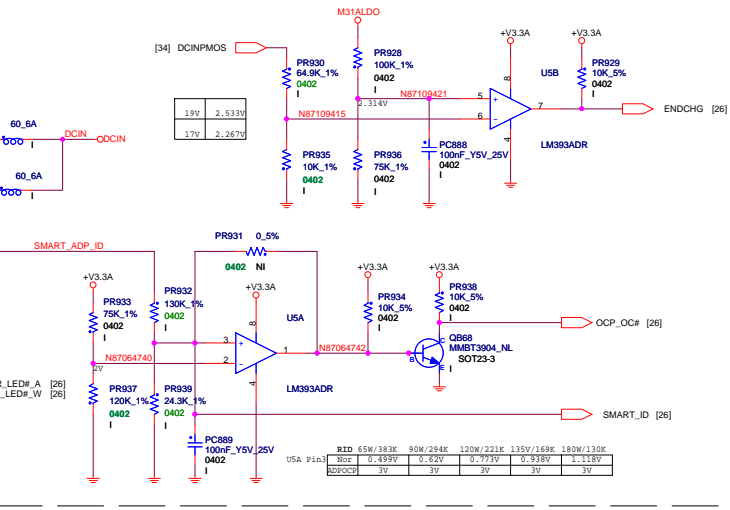
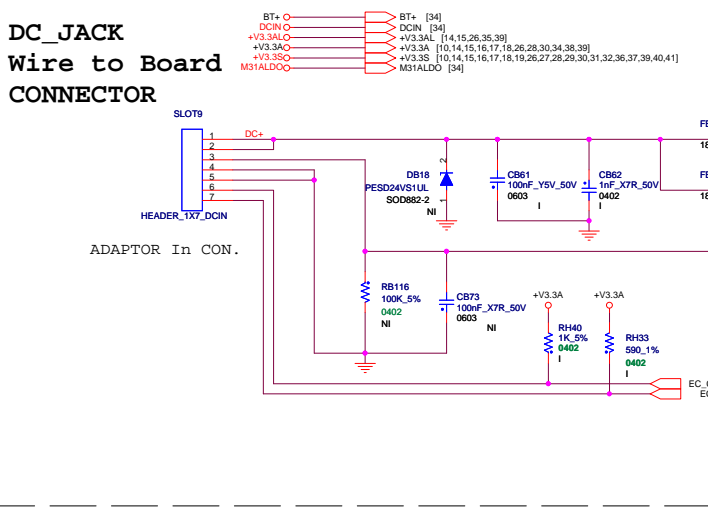
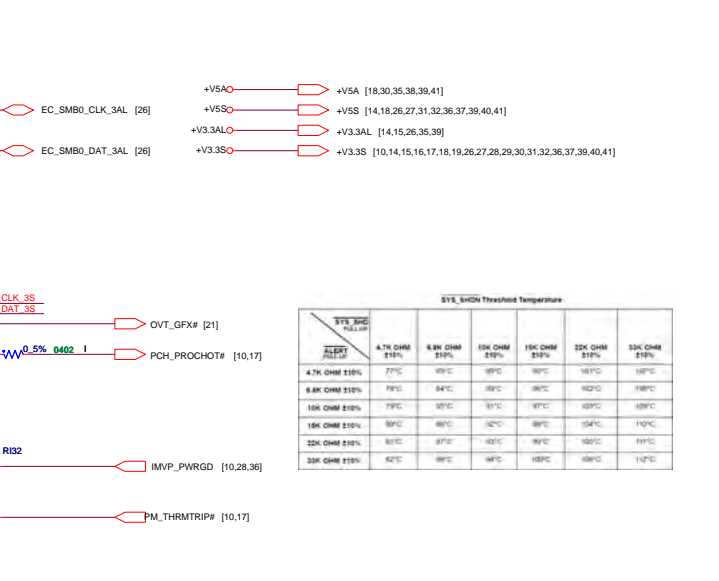
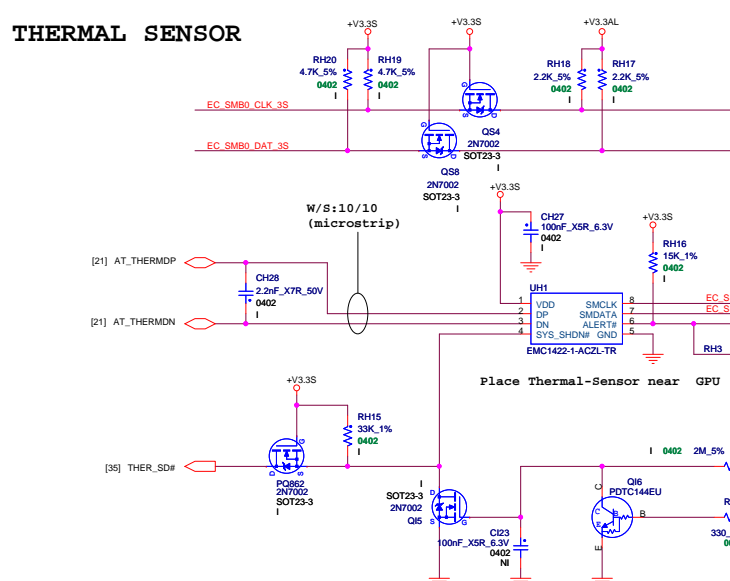
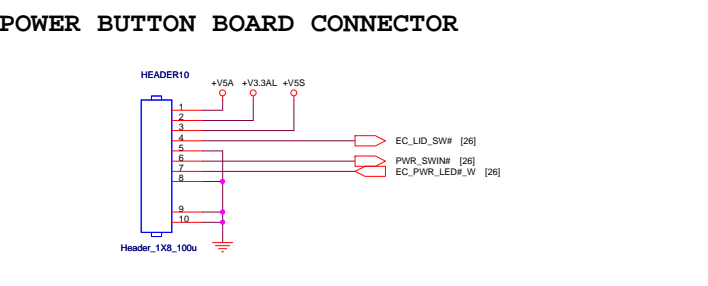
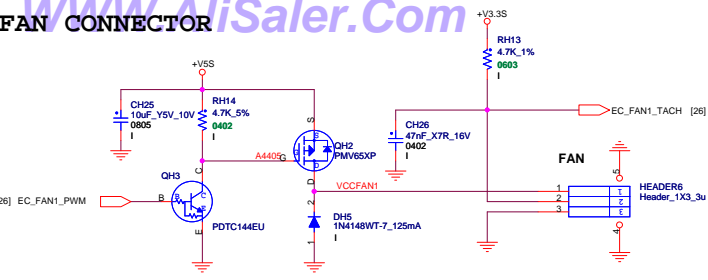


Discrete GPU: Install
UMA: Not Install



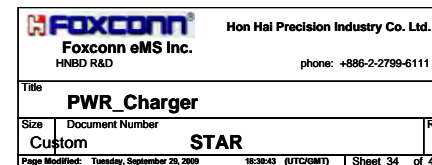
Discrete GPU:Not Install
UMA:Install

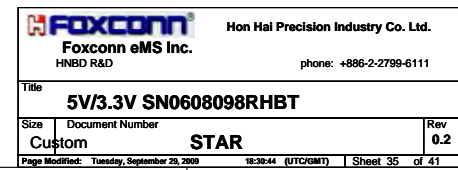


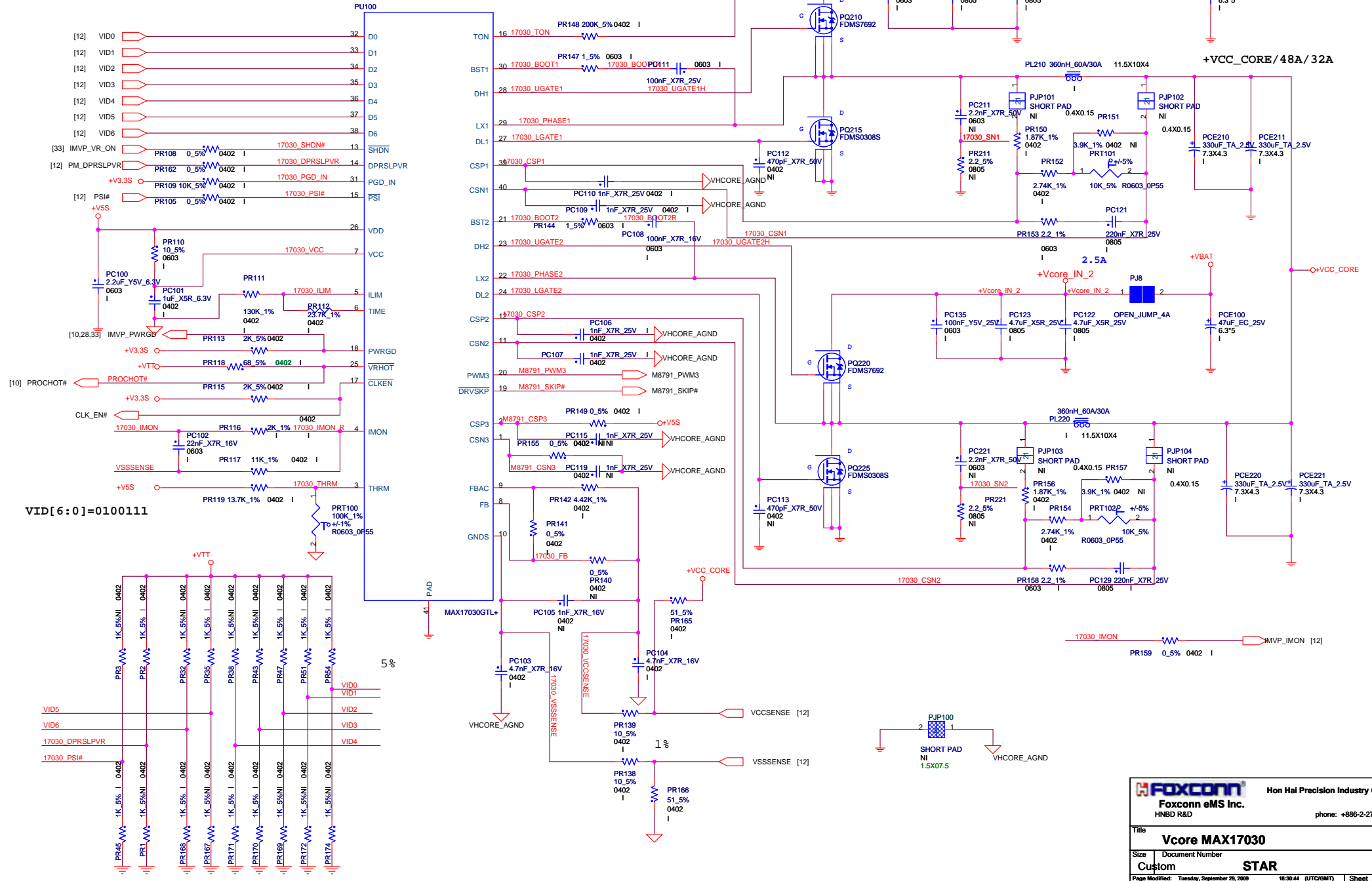


S7E SMC Threshold Temperature		4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C
6.8K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C
10K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C
15K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C
22K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C
33K OHM ±10%	77°C	77°C	77°C	77°C	77°C	77°C	77°C

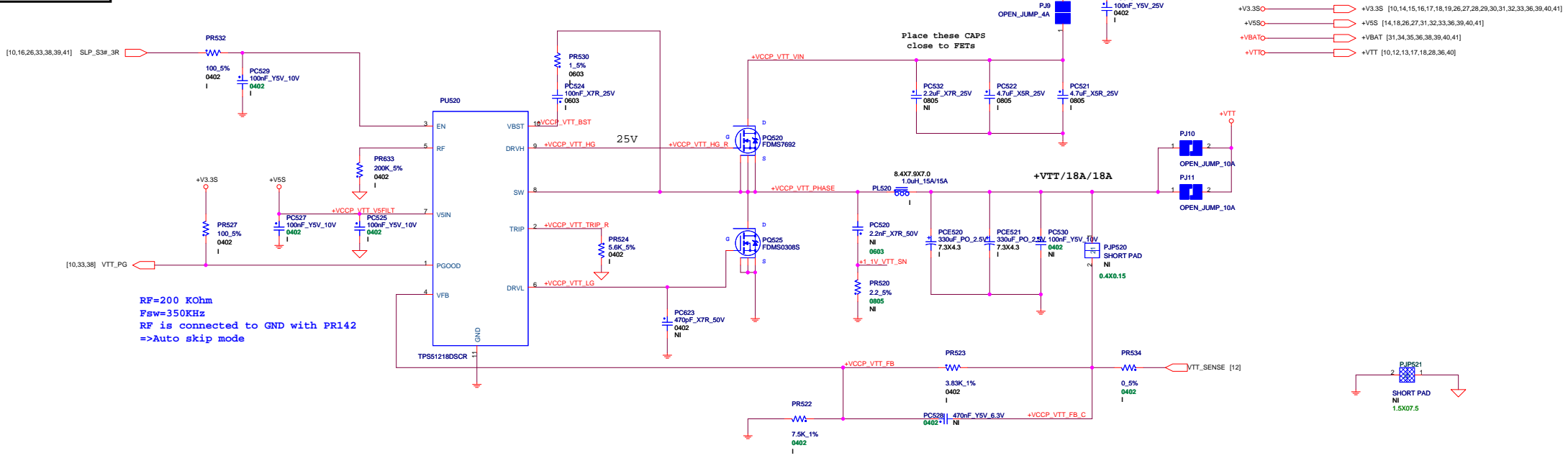
Pin No.	Symbol	Comments
1	BATT+	Batt., Battery Positive Terminal.
2	BATT+	Batt., Battery Positive Terminal.
3	IMD	IMD data interface I/O pin.
4	SMC	SMC data interface I/O pin.
5	ID	Open
6	b/i	Connect to thermistor (103AT2 equivalent)
7	GND	Batt., Battery Negative Terminal
8	GND	Batt., Battery Negative Terminal



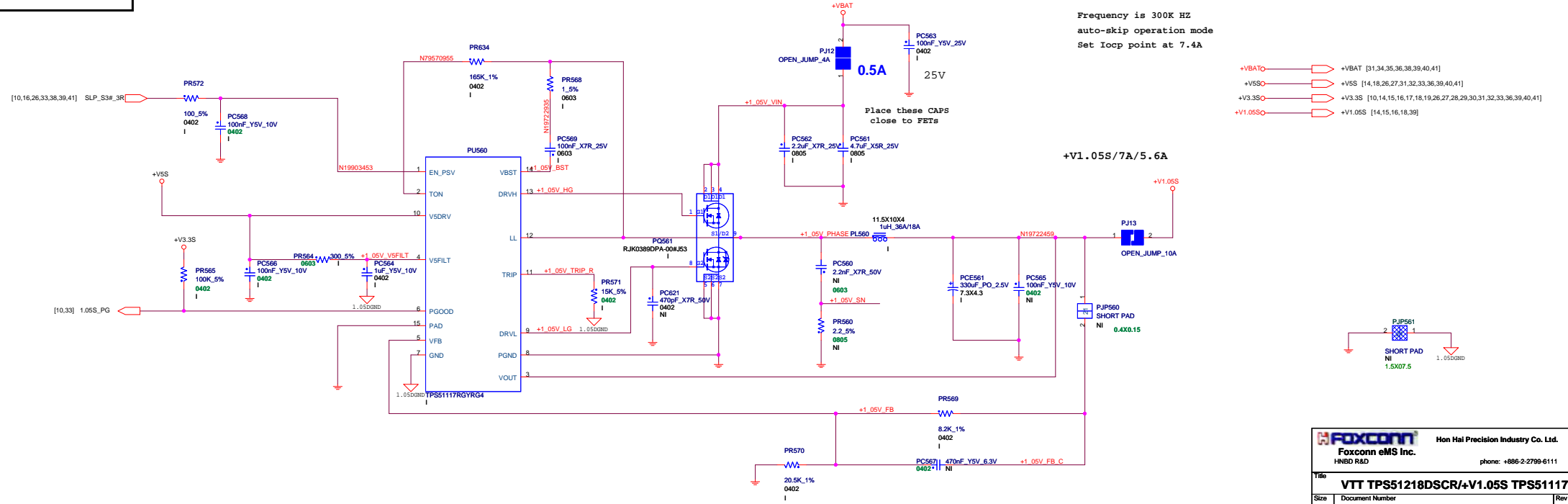


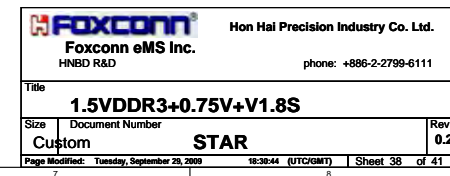


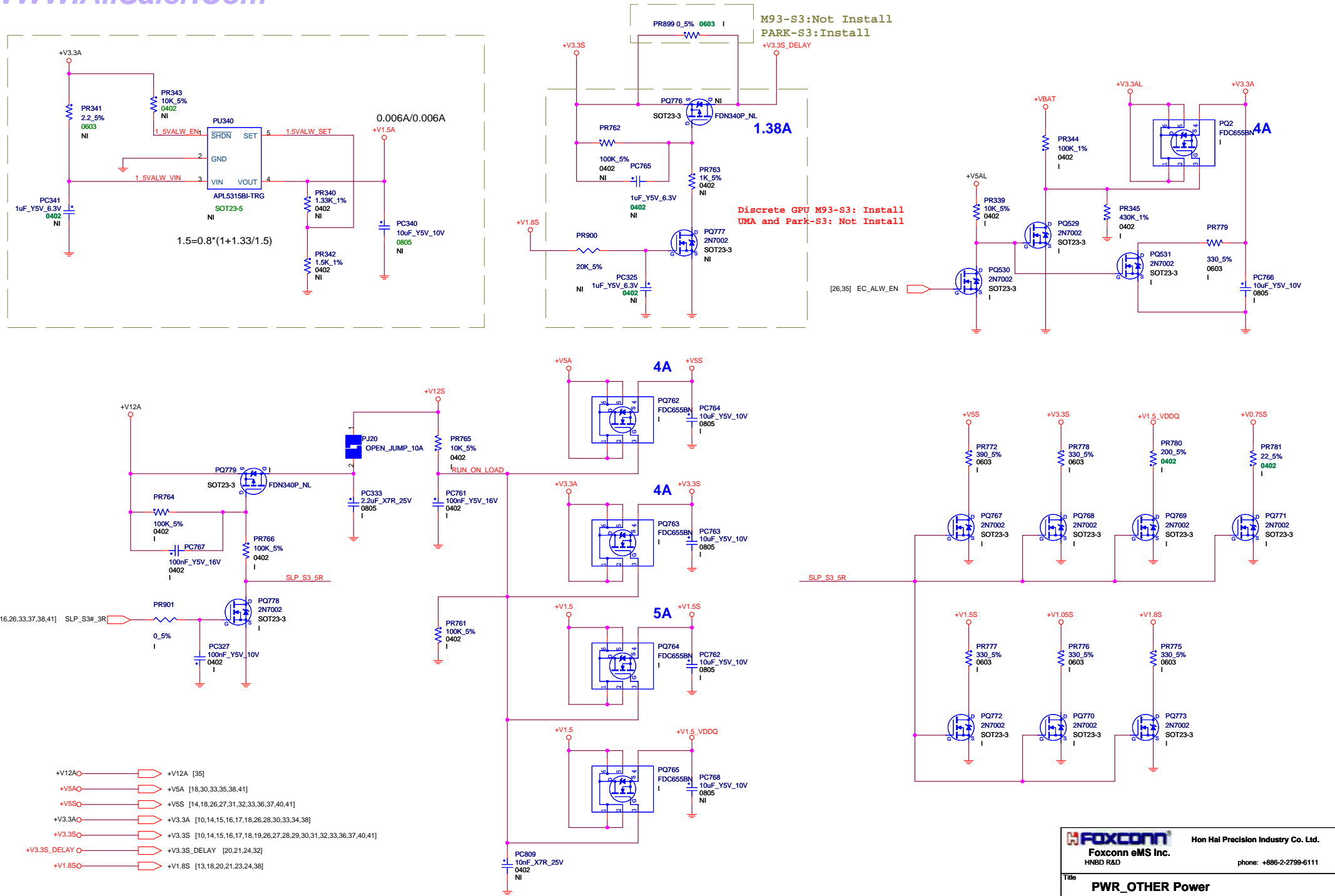
+VTT TPS51218



+V1.05S TPS51117

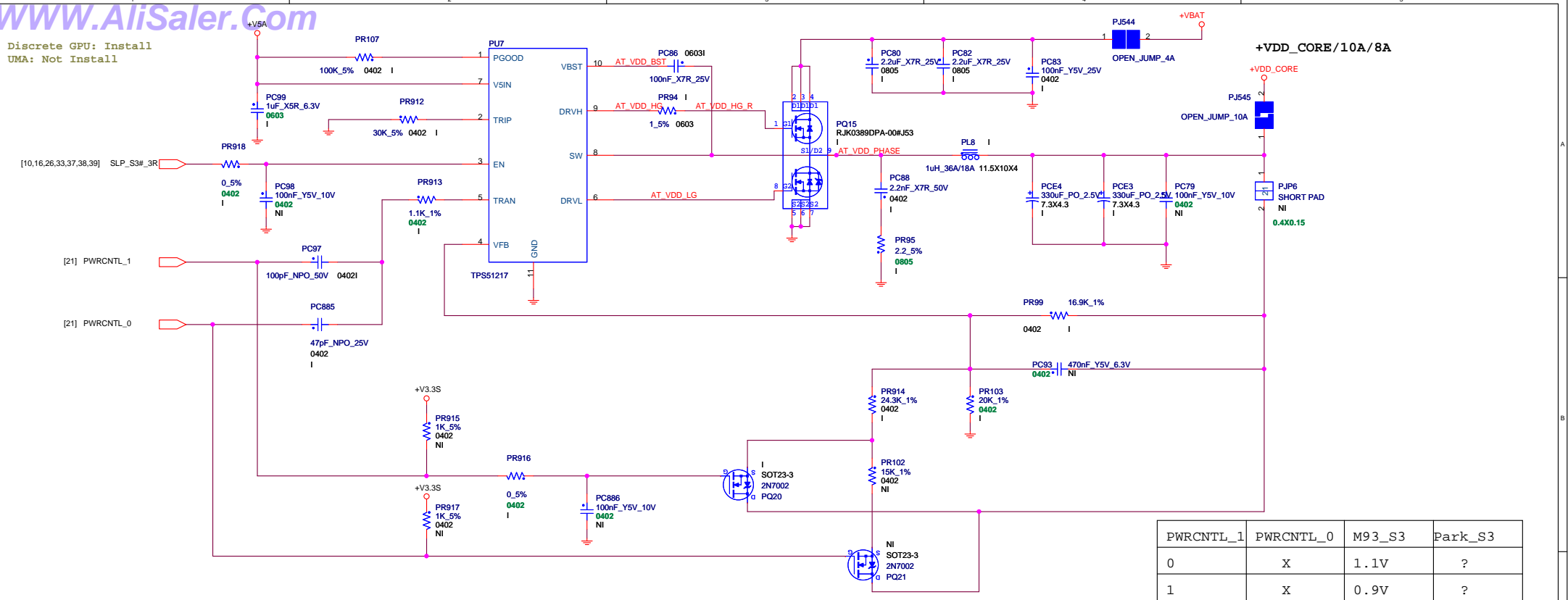








Discrete GPU: Install
UMA: Not Install



Discrete GPU: Install
UMA: Not Install

